Calhoun
Institutional Archive of the Naval Postgraduate School

Calhoun: The NPS Institutional Archive

DSpace Repository

Theses and Dissertations 1. Thesis and Dissertation Collection, all items

1959

Digital wave synthesis and pulse width modulation in an inverter power supply.

Arnold, James M.

http://hdl.handle.net/10945/14069

Downloaded from NPS Archive: Calhoun

DUDLEY
KNOX
LIBRARY

http://www.nps.edu/library

Calhoun is the Naval Postgraduate School's public access digital repository for research materials and institutional publications created by the NPS community. Calhoun is named for Professor of Mathematics Guy K. Calhoun, NPS's first appointed -- and published -- scholarly author.

Dudley Knox Library / Naval Postgraduate School
411 Dyer Road / 1 University Circle
Monterey, California USA 93943

NPS ARCHIVE
1959
ARNOLD, J.

DIGITAL WAVE SYNTHESIS AND PULSE WIDTH MODULATION IN AN INVERTER POWER SUPPLY

JAMES M. ARNOLD

Library
U. S. Naval Postgraduate School
Monterey, California

DUDLEY KNOX LIBRARY
NAVAL POSTGRADUATE SCHOOL
MONTEREY, CA 93943-5101

[redacted]

DIGITAL WAVE SYNTHESIS AND PULSE WIDTH MODULATION IN AN INVERTER POWER SUPPLY.

by

James M.Arnold

Commander,United States Navy

United States Naval Postgraduate School

Monterey,California

1959

Thesis
~~A7258~~

NPS ARCHIVE
1959
ARNOLD, J.

Library
U. S. Naval Postgraduate School
Monterey, California

DUDLEY KNOX LIBRARY
NAVAL POSTGRADUATE SCHOOL
MONTEREY, CA 93943-5101

NOTICE

[redacted]

Abstract

The second summer of the Ordnance Engineering, Guided Missiles, curriculum at the Naval Postgraduate School is devoted to an Industrial Experience Tour. The author was privileged to spend this period with the Lockheed Missiles and Space Division participating in the development of an inverter power supply for space satellites. Coordination of the tour and security clearance were handled by the office of the Naval Inspector of Ordnance, Sunnyvale, California.

Within the Communications Research Techniques Department, a team of five Lockheed engineers was assigned to this project. It was to this team that the author was attached. Preliminary investigation of the problem had already begun on one June when the tour commenced. At the time of this writing the inverter is nearing readiness for production.

The requirement was for a compact, lightweight inverter of exceptional efficiency and reliability. The primary power source may be a conventional storage battery or, eventually, solar or fuel cells.

Unusual specifications and design features include: (a) Input dc voltage range from 22 to 30 volts. (b) Minimum efficiency and power factor 85% and 0.8, respectively, over an output range of 50 to 500 watts of three-phase power. (c) Output voltage regulation within one percent

of 115 volts. (d) Frequency stability within 0.02% of 400 cycles per second. (e) Maximum five per cent distortion as compared to a pure sine wave. (f) Use of a recently announced solid state device, the Silicon Controlled-Rectifier, for rapid switching of substantial currents. (g) Synthesis of the desired sine wave by digital logic techniques. (h) Output voltage regulation by pulse width modulation. (i) Complete short-circuit protection.

Appreciation is expressed for the guidance and assistance provided by Dr.C.Rothauge of the Postgraduate School; also, Dr. Muehlner, Mr. Stewart, Mr. Kearns and Mr. Biggerstaff, all of the Lockheed Corporation.

Table of Contents

Section	Title	Page
I	Introduction	1
II	Analysis of a Typical Existing Inverter	2
III	Digital Logic for Synthesizing a Sine Wave via Step Functions	5
IV	Voltage Regulation by Pulse Width Modulation	19
V	Power Switching by Silicon Controlled Rectifiers	31
VI	Short Circuit Protection	46
VII	Conclusions	48
	Bibliography	51

List of Illustrations

Figure		Page
1.	Block Diagram of a Typical Existing Inverter	2
2.	Twelve Step Synthesis of a Sine Wave	5
3.	Output Stage for Twelve Step Wave	8
4.	Digital Logic Circuitry for Twelve Step Wave	9
5.	Delayed Square Wave Synthesis	11
6.	19.2 Kilocycle Crystal Clock	13
7.	Waveforms for Synchronizing Pulse Width Modulators and Corresponding Unfiltered Inverter Outputs	14
8.	Countdown Multivibrator	15
9.	Ring Counter Block Diagram and Truth Table	16
10.	Ring Counter Schematic Diagram	18
11.	Basic Saturable-Core Square Wave Oscillator	20
12.	Saturable-Core Square Wave Oscillator with Width Modulation	21
13.	Magnetic Pulse Width Modulator	23
14.	Waveforms of Magnetic Pulse Width Modulator and Output Stage	24
15.	Digital Logic Separation of Switching Pulses	24
16.	D.C. Feedback Amplifier for Pulse Width Modulator	25
17.	Experimental Transistorized Pulse Width Modulator	27
18.	Transistorized Pulse Width Modulator and Waveforms	29
19.	D.C. Feedback Amplifier for Transistorized Pulse Width Modulator	30

Figure		Page
20.	Principles of Silicon Controlled-Rectifier Operation	32
21.	Functional Characteristics of Silicon Controlled-Rectifier	34
22.	Operational Characteristics of Silicon Controlled-Rectifier	34
23.	Typical Operation of Silicon Controlled-Rectifier	34
24.	Silicon Controlled-Rectifier Biased in Conducting State	37
25.	Shunt-Capacitor Rectifier Turn-off Circuit	38
26.	Experimental Output Stage	39
27.	Single Phase Output Stage	41
28.	Blocking-Oscillator Driver	42
29.	Output Filter	43
30.	Curves of Efficiency and Power Losses Versus Load	44
31.	Output Stage Waveforms	45
32.	Short Circuit Protective Circuit	46
33.	Eight Step Sine Wave Synthesis	48
34.	Overall Block Diagram of Inverter	50

I

Introduction

In a satellite currently under development, the requirement for repeated starting of several three-phase hysteresis synchronous motors, where only low voltage, direct current power was available, indicated the necessity for design of a special inverter power supply. Several more conventional items of single and three-phase load are also to be supported by this supply.

The primary source of power will probably eventually be solar or fuel cells, or some advanced form of storage battery. The voltage of the source may be expected to vary between 22 and 30 volts, but 28 volts will be considered nominal.

Required power output also has a wide range; 50 to 500 watts. Voltage and frequency regulation are to be relatively close; 1% from 115 volts and .02% from 100 cycles, respectively. Efficiency and reliability must be exceptionally high. Environmental conditions of shock, vibration, temperature, etc. are definitely more severe than in usual land installations.

The approach to the design problem was made via analysis of existing inverters, study of digital logic techniques for voltage regulation, and investigation of Silicon Controlled-Rectifier characteristics for use as power switches.

II

Analysis of a Typical Existing Inverter

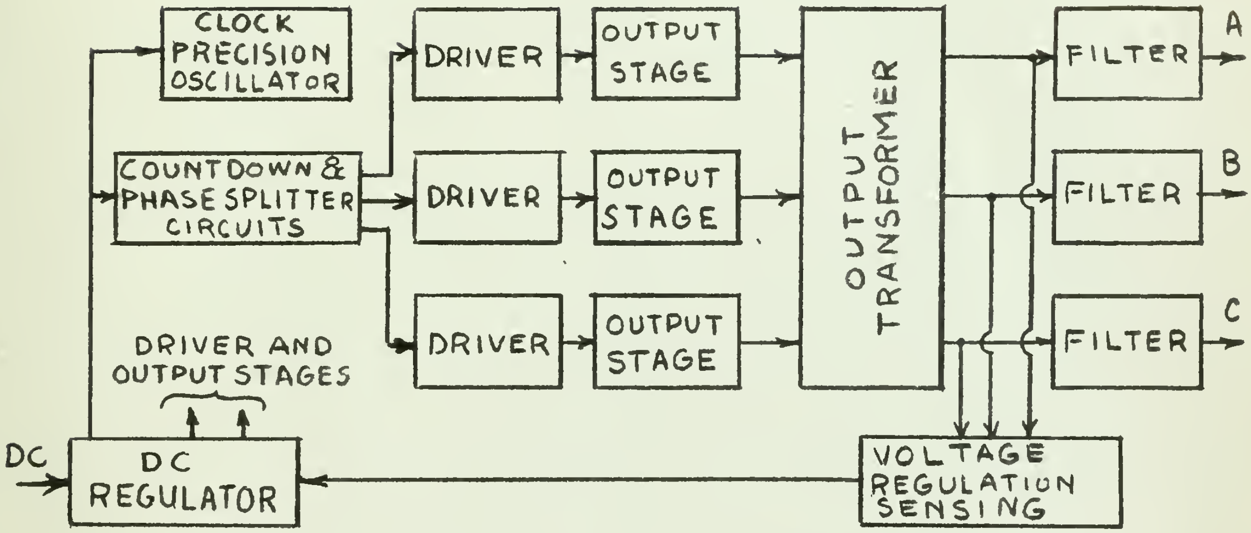


Fig. 1 Block Diagram of a Typical Existing Inverter

In this commercially available inverter, a sine wave is generated by a crystal controlled oscillator, or 'clock'. From this wave are generated three-phase square waves by means of counting down, phase splitting, and wave squaring. These square waves are amplified in drivers and power transistor output switches. Filters, of which the output transformer secondary may be a part, remove the harmonics to provide sine wave power. Output voltage is compared with a zener diode reference and used to control the d.c. regulator by on-off time-modulation of the germanium power transistors therein.

Considerable power is lost in this system; major sources of loss are the D. C. regulator, driver stage, and output filters.

D. C. regulator loss is due to the relatively heavy currents flowing in the germanium transistors, even though their forward resistance when operating in the 'switching' mode is low.

Driver stages also operate in a switching mode as the square wave input drives them alternately from cutoff to saturation. Both the power loss within the drivers and their power output, which is dissipated as the base drive for the output stages, are significant; particularly when considering efficiency at minimum loads.

Output filter loss is due largely to the approximate 20% harmonic content of the square waveform.

An example of this type of inverter was procured and tested for efficiency. Losses in the various sections when operated at 25% of its 200 watt rating were:

Section of Inverter	Watts loss
Count Down	1.2
Voltage Sensing	1.8
Regulators	5.0
Drivers	3.3
Power Stages and Filters	14.5
Total	25.8

$$\text{Hence efficiency } (\eta) \quad \frac{\text{Load}}{\text{Load + Losses}} \quad \frac{50}{75.8} \quad 66\%$$

This is in striking contrast with the 85% efficiency specified for the proposed system.

As a point of departure, this inverter nevertheless includes several features considered essential. For accurate frequency and inter-phase relation control, a precision oscillator running at at least three times the output frequency is required. Therefore, a crystal oscillator will be used. Practical crystal oscillators have a much higher frequency than theabove minimum (1200 cycles in a 400 cycle system), so that some countdown system must be used.

Filters will continue to be necessary for anything less than a pure sine wave form delivered at the secondary of the output transformer. As this is impractical, some form of sine wave synthesis having a lower harmonic content than the simple square wave but attainable by relatively simple circuitry is indicated. Naturally, the filter used must be designed for maximum efficiency.

The current-switching function, performed by germanium power transistors here, can be handled with much less drive power by the newly announced Silicon Controlled-Rectifier; a four layer, solid-state device having characteristics somewhat similar to a thyratron.

Finally, it appears that some other means of voltage regulation than a series method operating on the input dc supply will be necessary. Since digital logic is contemplated for synthesizing the desired sine wave as a series of steps, width modulation of the top step, (thus varying effective voltage) seems attractive. It is contemplated that output voltage variations due to varying supply voltage, or varying load, can be compensated for by this method.

III

Digital Logic for Synthesizing a Sine Wave Via Step Functions

Application notes provided by the manufacturer indicate that the Silicon Controlled-Rectifier can be turned on and off via short pulses in proper time sequence. Thus we are naturally led to digital logic techniques.

The first sinusoid synthesis analyzed was a twelve step waveform as shown in Fig. 2.

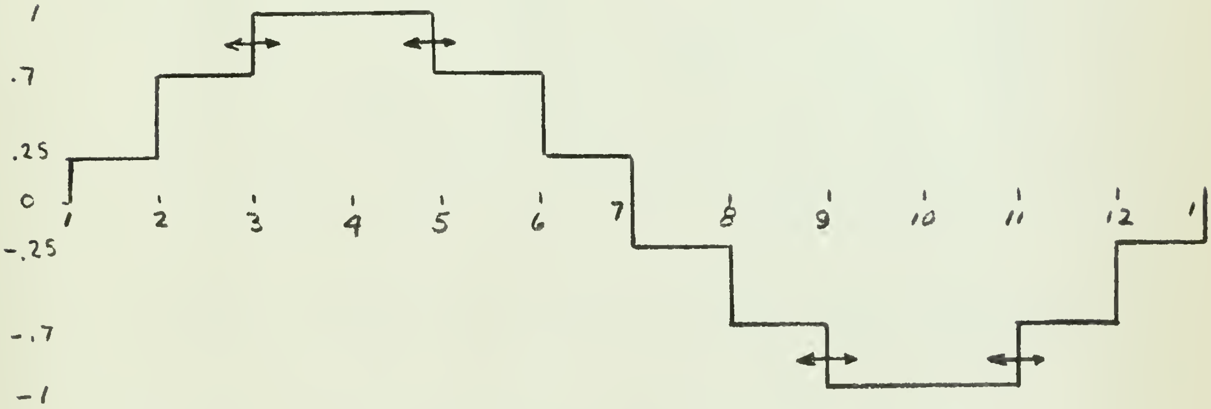


Fig. 2 Twelve Step Synthesis of a Sine Wave

Step amplitudes of 25%, 70%, and 100% of maximum current are to be attained by six Silicon Controlled-Rectifiers (SCR's) and taps on a transformer primary. Each step is to have a duration of some multiple of one-twelfth cycle except that the width of the top and bottom steps should be **variable**, i.e. that times three, five, nine, and eleven can be advanced or retarded as shown. The extremes of such varia-

tion are the cases where there is no 70% step and where there is no 100% step.

A Fourier analysis of this waveform for the unmodulated case (top step has duration of one sixth cycle) was performed. This analysis was commenced at the center of the top step and extended only through one-fourth cycle due to symmetry. Only odd harmonics will be present as $f(x) = -f(x+\frac{T}{2})$.

$$A_n = \frac{2}{T}\int_0^T f(x)\cos\frac{2n\pi x}{T}\,dx$$

$B_n = 0$ as function is odd.

$$A_n = \frac{8}{T}\int_0^{T/4} f(x)\cos\frac{2n\pi x}{T}\,dx \quad \text{where } f(x) = \begin{cases} 1 & 0 < x < \frac{T}{12} \\ .7 & \frac{T}{12} < x < \frac{T}{6} \\ .25 & \frac{T}{6} < x < \frac{T}{4} \end{cases}$$

$$= \frac{8}{T}\left[\int_0^{T/12}\cos\frac{2n\pi x}{T}\,dx + \int_{T/12}^{T/6}.7\cos\frac{2n\pi x}{T}\,dx + \int_{T/6}^{T/4}.25\cos\frac{2n\pi x}{T}\,dx\right]$$

$$= \frac{8}{\cancel{T}}\,\frac{\cancel{T}}{2n\pi}\left[\sin\frac{2n\pi x}{T}\Big|_0^{T/12} + .7\sin\frac{2n\pi x}{T}\Big|_{T/12}^{T/6} + .25\sin\frac{2n\pi x}{T}\Big|_{T/6}^{T/4}\right]$$

$$= \frac{4}{n\pi}\left\{1(.5-0) + .7(.867-.5) + .25(1-.867)\right\}$$

$$= \frac{4}{n\pi}(.5 + .2569 + .0332)$$

$$= \frac{4}{n\pi}(.7901) \underset{n \rightarrow 1}{=} 1.006$$

Relative fundamental power $(P_1) = \frac{(1.006)^2}{2} = .507$

Total power $(P_T) = \frac{4}{T}\left\{(1)^2\frac{T}{12} + (.7)^2\frac{T}{12} + (.25)^2\frac{T}{12}\right\} = .5175$

Percent of P_T in $P_1 = \frac{100 P_1}{P_T} = \frac{50.7}{.5175} = 97.97\%$

Relative powers in each odd harmonic up to the 15th were computed to determine the nature of the filtering problem and are tabulated herewith. Corresponding values for a square wave are included for comparison.

n	$4/n\pi$	A_n	$A_n rms$	$(A_n rms)^2$	$\% P_T$	$\% P_T$ (sq wave)
1	1.272	1.00000	.7116	.5064	97.735	81
3	.424	.02120	.0149	.00022	.0435	8.9
5	.254	.00254	.0018	.0000032	.0006	3.2
7	.182	-.00182	-.0013	.0000017	.0003	1.64
9	.142	-.00710	-.005	.000025	.0004	1
11	.110	-.09150	-.0647	.0042	.8106	.61
13	.098	.07740	.0547	.003	.579	.48
15	.036	.0043	.003	.000009	.0017	.36

It is noted that the only significant harmonics are the 11th and 13th and are easily filterable.

Similar analyses were performed for the extreme width modulation cases:

	Max. Width (no 70% step)				Min. Width (no 100% step)			
n	A_n	$A_n rms$	$(A_n rms)^2$	$\% P_T$	A_n	$A_n rms$	$(A_n rms)^2$	$\% P_T$
1	1.15	.813	.66	95.85	.815	.576	.532	95.56
3	-.106	-.075	.0056	.812	.106	-.075	.0056	1.613
5	-.1016	-.072	.0052	.754	-.036	-.025	.0006	.173
7	.0728	.052	.0027	.391	.0025	.018	.0003	.086
9	.0355	.025	.0006	.087	.036	.025	.0006	.173
11	-.1045	-.074	.0055	.797	.074	.052	.0027	.778
13	.0882	.062	.0038	.551	.063	.045	.002	.576
15	-.0215	-.015	.0002	.029	.022	.016	.0002	.058

Note: The filtering problems here are appreciably worse but with 5% distortion allowed and the expectation that extreme modulation will not be required, the synthesis remains acceptable.

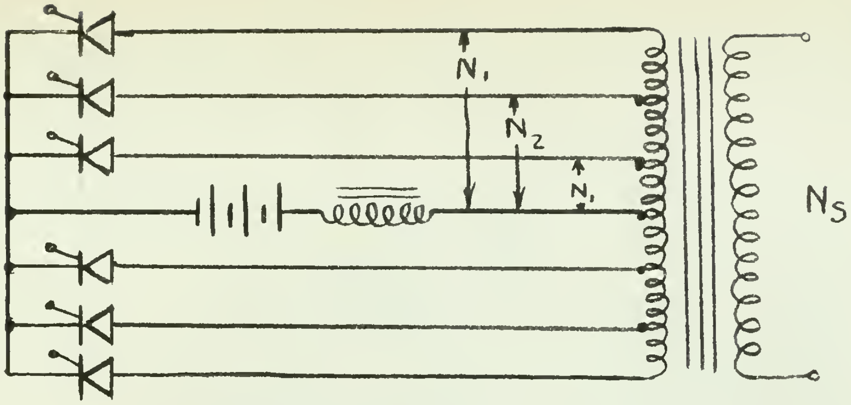


Fig. 3 Output Stage for Twelve Step Wave

With the controlled rectifiers and tapped transformer shown in Fig. 3, the desired wave form requires the following switching sequence:

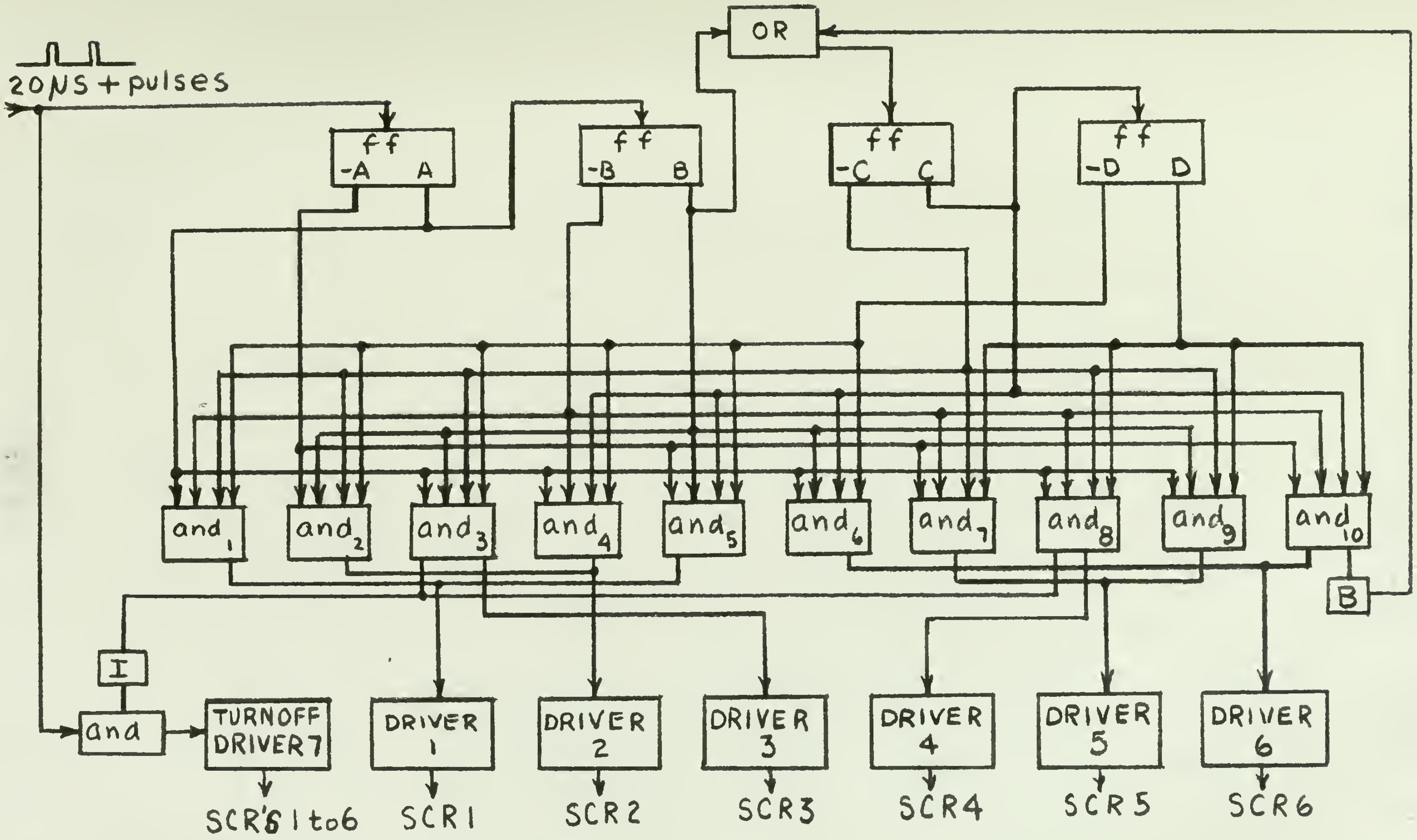
Time	1	2	3*	4	5*	6	7	8	9*	10	11*	12
Rectifier turn-on	1	2	3	-	2	1	6	5	4	-	5	6
Rectifier turn-off	6	1	2	-	3	2	1	6	5	-	4	5

(* times variable by pulse width modulation)

Specifications for the Silicon Controlled-Rectifier state that a pulse with minimums of three volts, 80 milliamps, and two microseconds will serve as a turn-on pulse under the worst possible conditions. Therefore, as SCR drivers, a set of six blocking oscillators capable of delivering four volt, 100 ma., 15 microsecond pulses were contemplated. A seventh, common turn-off driver will also be required. These drivers require a pattern of triggers as follows:

Driver	1	2	3	4	5	6	7
time	1&6	2&5	3	9	8&11	7&12	1to12

The digital logic circuit designed to provide these triggers is shown in Fig. 4. Essentially it is a four-stage binary counter (four flip-flops) and a diode matrix. This



Symbols: and=diode'and'gate, B=buffer amplifier, ff=flip-flop, I=inverter, OR=diode'or'gate

Fig. 4 Digital Logic Circuitry for 12 Step Wave

counter utilizes feedback arranged to cause a repetitive sequence of twelve counts. For laboratory testing a series of 20μs positive pulses from a pulse generator was substituted for the crystal clock. All turn-on pulses to drivers are coincident with the *trailing* edges of the 20μs pulses, whereas turn-off pulses occur at their *leading* edges, thus ensuring that no SCR turns on before the preceding one turns off.

Before committing this design concept to hardware it seemed advisable to construct and test actual circuitry for turning on and off the Silicon Controlled-Rectifiers; the manufacturers application sheets furnishing only 'suggested' circuits for these functions.

The considerable difficulties in achieving satisfactory turn-on and turn-off will be described in a later section. It will suffice to say here that the number of auxiliary components which appeared to be necessary, combined with the basic six SCR's, their six drivers, and the associated logic circuitry, (all to be tripled for a three phase system) strongly advocated a simpler wave synthesis with fewer components.

It was decided to determine whether a single pair of SCR's, the same number required to develop a square wave, could be utilized to produce a wave form with sufficient fundamental power to meet the 85% efficiency specification. The scheme selected was a "Four Step" or "Delayed square wave" as shown in Fig. 5.

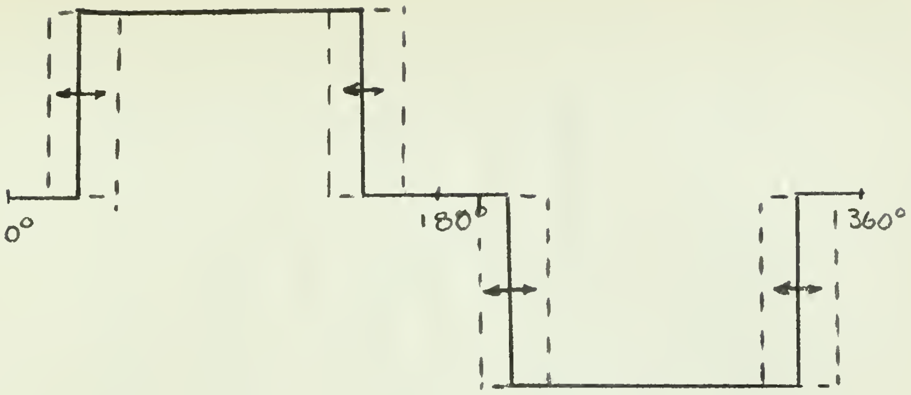


Fig. 5 "Delayed Square Wave" Synthesis

A Fourier analysis of this waveform for each of three cases was made. The cases were:

1. Nominal supply voltage (28 v) case, where the positive and negative excursions have twice the duration of the zero-level, 'delay' period.

2. Maximum supply voltage case (30 v) where the positive and negative excursions will be narrowed by one twenty-fourth of a cycle from the 'Nominal' case.

3. Minimum voltage (22 v) case where excursions are widened by one twenty fourth cycle.

The calculations for the 'Nominal' case and the tabulation for all three cases are as follows:

$$A_n = \frac{2}{T}\int_0^T f(x)\cos\frac{2n\pi x}{T}\,dx$$

$$= \frac{2}{T}\left[\int_0^{T/6}\cos\frac{2n\pi x}{T}\,dx - \int_{T/3}^{\frac{2T}{3}}\cos\frac{2n\pi x}{T}\,dx + \int_{\frac{5T}{6}}^{T}\cos\frac{2n\pi x}{T}\,dx\right]$$

$$= \frac{1}{n\pi}\left[\sin\frac{2n\pi x}{T}\Big|_0^{T/6} - \sin\frac{2n\pi x}{T}\Big|_{T/3}^{\frac{2T}{3}} + \sin\frac{2n\pi x}{T}\Big|_{\frac{5T}{6}}^{T}\right]$$

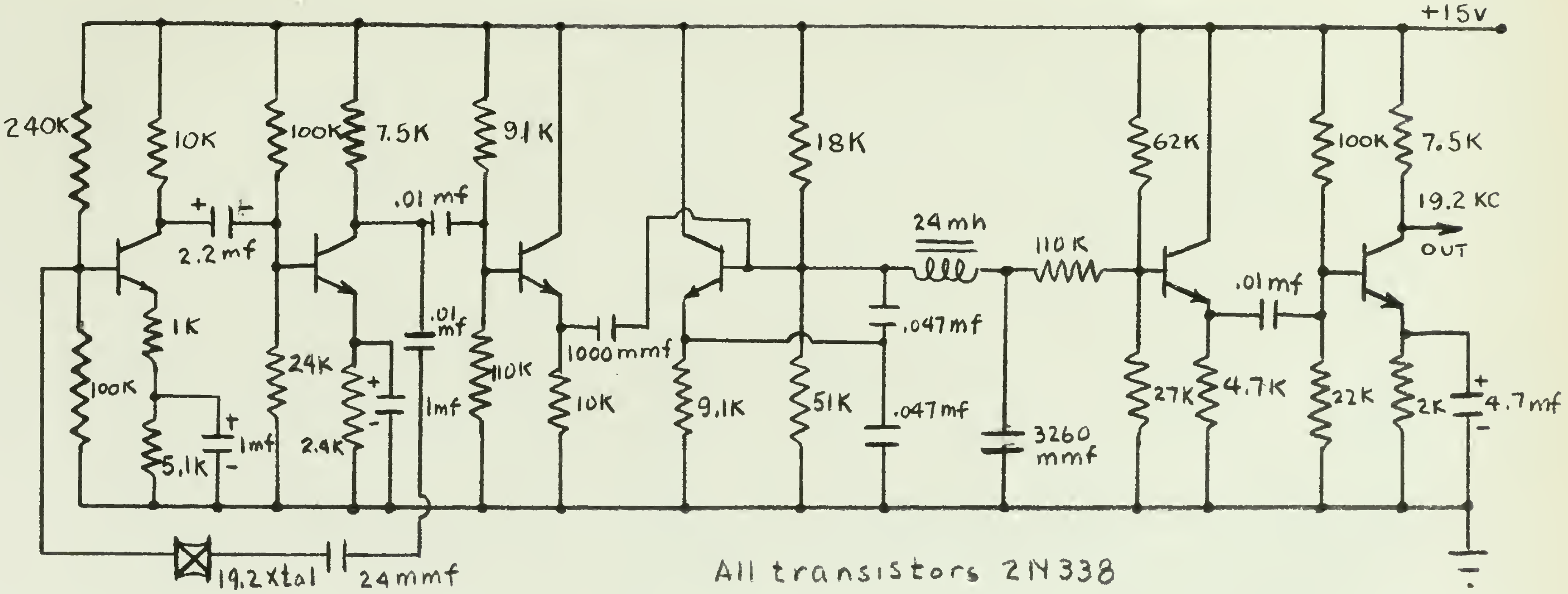
$$= \frac{1}{n\pi}\left[\sin(n60^\circ) - \sin(n240^\circ) + \sin(n120^\circ) - \sin(n300^\circ)\right]$$

Percent of Total Power in each Harmonic for each Case:

n	Case 1	Case 2	Case 3	Sq. Wave
1	91.02	80.82	90.62	81.
3	0	9.	5.4	8.9
5	3.65	6.24	.23	3.2
7	1.88	1.66	.13	1.64
9	0	1.	.6	1.
11	.75	.67	.75	.61
13	.54	.48	.54	.48
15	0	.37	.22	.36

That percentage of total power which is available at the fundamental frequency in this waveform is considered sufficient to justify developing digital logic circuitry therefor. The first problem is to determine the wave forms which must be delivered to the three pulse width modulators and to devise a scheme for obtaining them from the output of the clock. The frequency of the clock was set at 19.2 kilocycles (the 48th harmonic of 400 cycles) as there was a stable transistorized circuit already available at that frequency; also, that frequency is the product of 400 and a multiple of three, thus adapting it to a three-phase system. The crystal oscillator clock circuit shown in Fig. 6 includes a standby LC oscillator which automatically takes over in case of failure, providing a source of only slightly less stability.

As will be explained later, an 800 cycle wave train is required to synchronize each pulse width modulator. Thus, three such waves differing in phase by 120 degrees will be developed. These waves, referred to as X, Y, and Z, are



All transistors 2N338

Fig. 6 19.2 Kc. Crystal Clock

shown in Fig. 7 with their corresponding inverter output waveforms.

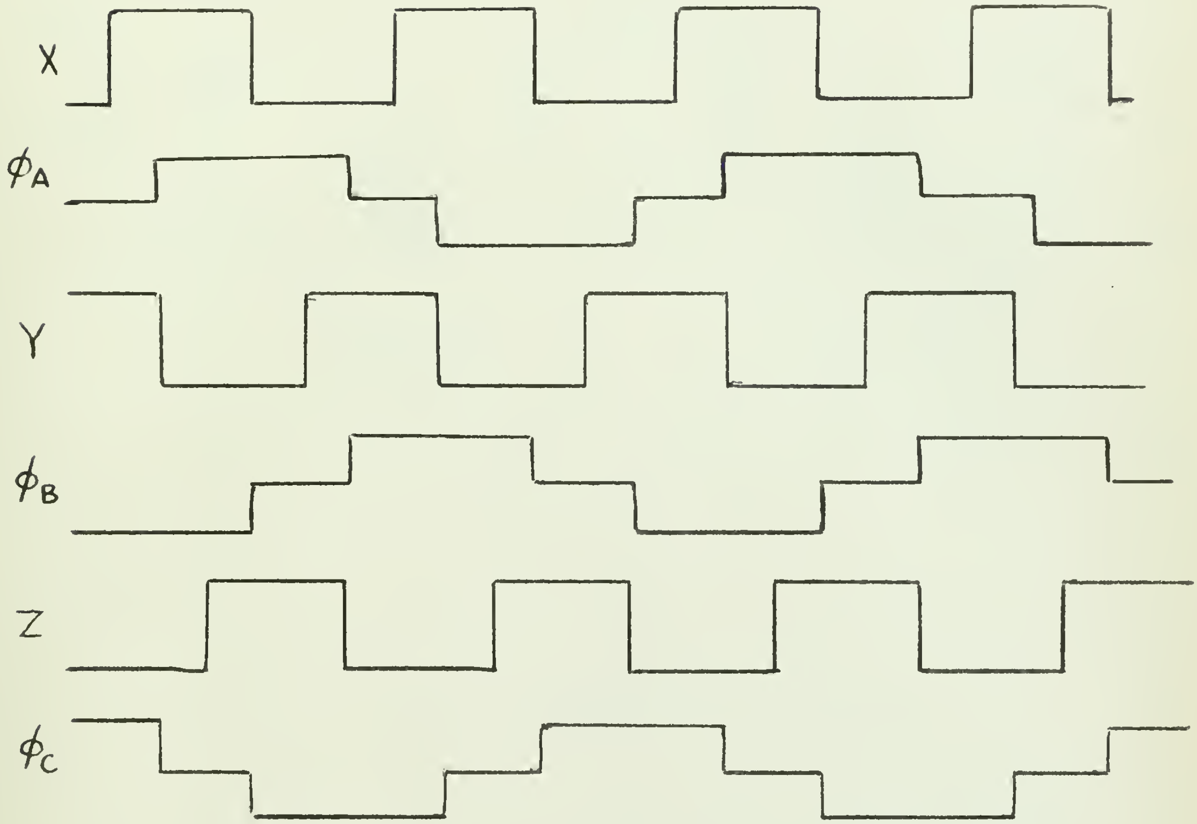


Fig. 7 Waveforms for Synchronizing Pulse Width Modulators and Corresponding Unfiltered Inverter Outputs

The approach to developing the necessary logic circuitry commences with writing a 'Truth Table' listing the binary 0 or 1 conditions for the three waves at one-sixth cycle intervals. This spacing is due to the fact that there is an 'event'; specifically, a rise or fall, occurring every one-sixth of a cycle. This fact implies that an input to the proposed logic circuit having a frequency of six times 400, or 4.8 KC, is required. This frequency is had by two cascaded countdown multivibrators (as shown in Fig. 8) following the clock.

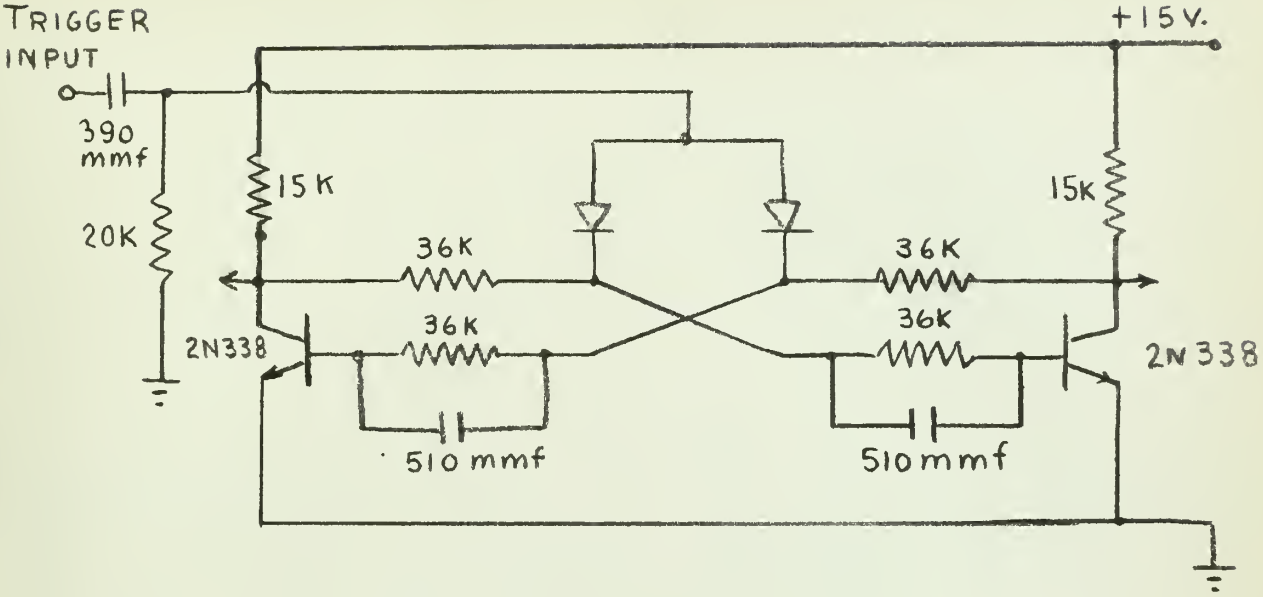


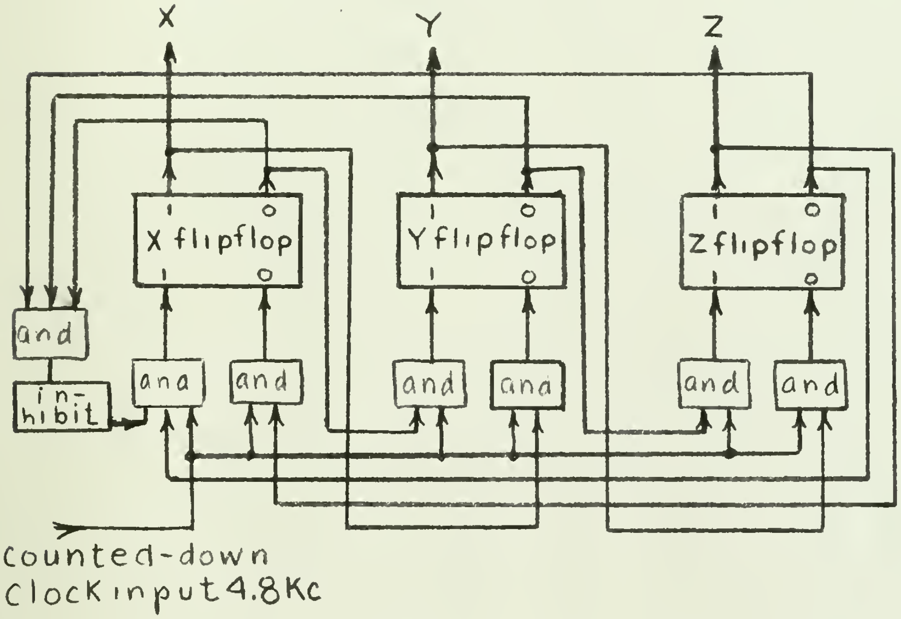
Fig. 8 Countdown Multivibrator

The basic element to be used in the logic circuitry is a binary choice circuit, (0 or 1), or "flip-flop". To form the required six combinations of 0 and 1, it is necessary to form eight combinations and reject two of them. Further, some means of feedback between the various flip-flops is required to establish and maintain the desired cyclic sequence. Three flip-flops are required as they produce binary combinations in numbers equal to that 'power of two' represented by the number of flip-flops.

A characteristic of the flip-flop is that it will remain in either the 0 (or 1) condition until a 1 (or 0) input causes it to reverse. The truth table and a digital logic circuit capable of producing the binary number combinations listed in

that table are shown in Fig. 9.

Operation of the logic circuit is as follows: 4.8 KC clock pulses 'enable' all X, Y, and Z 'and' circuits at every such pulse. Assume that the three flip-flops are initially in any one of eight combinations of conditions except 000 and 111 (there being no instant when waves X, Y, and Z are all to be off or on).



TRUTH TABLE

time	X	Y	Z
6	0	1	0
1	1	1	0
2	1	0	0
3	1	0	1
4	0	0	1
5	0	1	1 ←
6	0	1	0
1	1	1	0

(combinations 000 and 111 rejected)

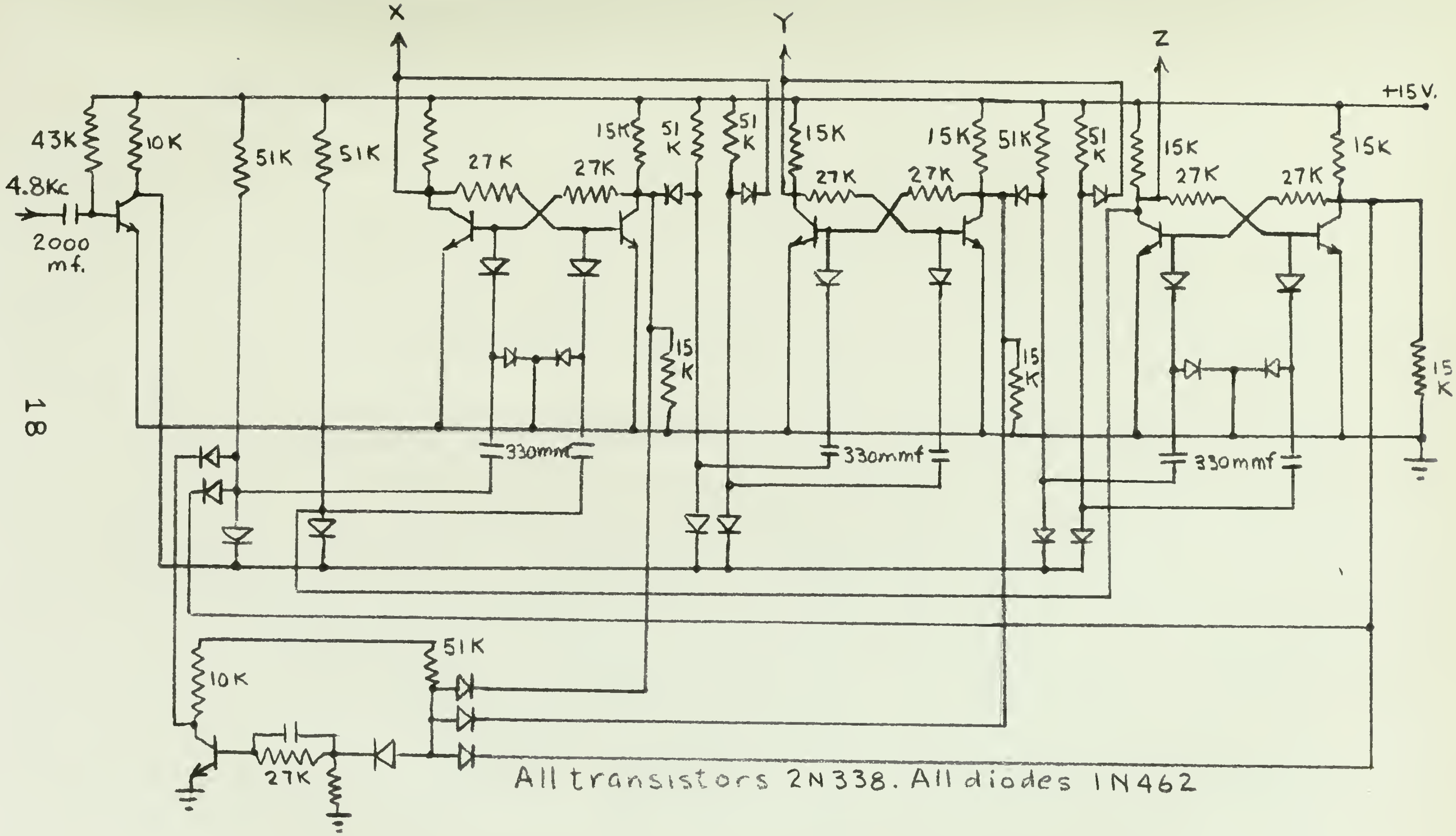
Fig. 9 Ring Counter Block Diagram and Truth Table

At the instant of the trailing edge of the first clock pulse to arrive, the flip-flops will assume the next combination of states in the truth table, and so on, cyclically. In the event that the combination (000) exists initially, the "and" and "inhibit" circuits, shown together at the lower left, function to set up combination number 5, ie. (011). If combination (111) exists initially, these circuits set up (000), then (011), as before.

A schematic of the 'Ring Counter' (so called because of

the feedback arrangement and cyclic operation) is shown in Fig. 1 .

The three phase square waves X, Y, and Z are at 800 cycles and are applied to the three pulse width modulators. Additional digital logic circuitry will follow the pulse width modulators to 'sort out' the time-varying pulses required for triggering the drivers which gate the Silicon Controlled-Rectifiers. This additional logic will be described in the next section in conjunction with the development of two types of pulse width modulator.



All transistors 2N338. All diodes IN462

FIG. 10 RING COUNTER

IV

Voltage Regulation by Pulse Width Modulation

In the preceding section we saw that the area under a stepped wave, and thus its effective voltage, could be varied by varying the width of the top step. Three-phase square waves X, Y, and Z are of constant frequency as developed by clock and ring counter and thus do not provide the required variable width. The design of a variable pulse width modulator (PWM) which will produce a train of time-varying driver trigger pulses from waves X, Y, and Z will be described in this section.

The basic principle first selected was that of keying a saturable-core square-wave oscillator from either X, Y, or Z, then varying the width of its positive and negative excursions by means of saturable reactors. The width variation must be symmetrical about some central point to maintain accurate phase relationship between the three phases.

A basic saturable-core square wave oscillator is shown in Fig. 11. The principle of operation is as follows: The initial flow of current in the collector circuit of one transistor exceeds that flowing in the other and unbalanced currents flow in the two halves of the transformer primary. The effect of the heavier current in one half is to induce a voltage in the other half in such a direction as to bias the more heavily conducting transistor into even heavier conduction, when applied via a suitable resistor to its base. Simultaneously, a signal of opposite phase is connected to the

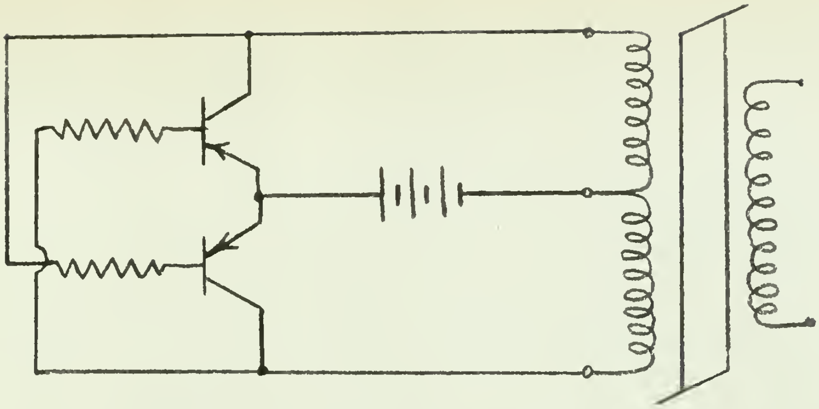


Fig. 11 Basic Saturable-Core Square Wave Oscillator

base of the more lightly conducting transistor to further reduce its conduction towards cut-off. This action is regenerative and continues until the transformer core saturates and the transformer can no longer maintain a rising collector current. At this time the currents reverse and the conducting transistor is cut off while the non-conducting unit is driven into conduction, and so on. The resulting output wave at the secondary is essentially square, with a repetition rate depending on: (a) supply voltage, (b) inductance of the primary and, (c) peak collector current drawn by the conducting transistor.

For purposes of design, frequency is controlled by varying: (a) the number of primary turns, (b) transformer core area and material and, (c) the feedback current.

The familiar principle of synchronizing a multivibrator by injection of a frequency slightly higher than its free running rate seemed feasible here, so the oscillator was designed to run at slightly less than 800 cycles at a supply voltage of fifteen volts. Incidentally, this value of 15 volts was

arbitrarily selected as the output voltage of a regulated dc power supply for all B+ requirements within the inverter control circuits. This choice was based on the ratings of the numerous transistors used and the lower limit of 22 volts to be expected from the primary power source.

For preliminary experimentation the oscillator was allowed to free-run during the development of the width modulation device.

The width modulation is to be provided by a pair of saturable reactors in series with the oscillator transformer secondary. The circuit design for oscillator with width modulator is shown in Fig. 12.

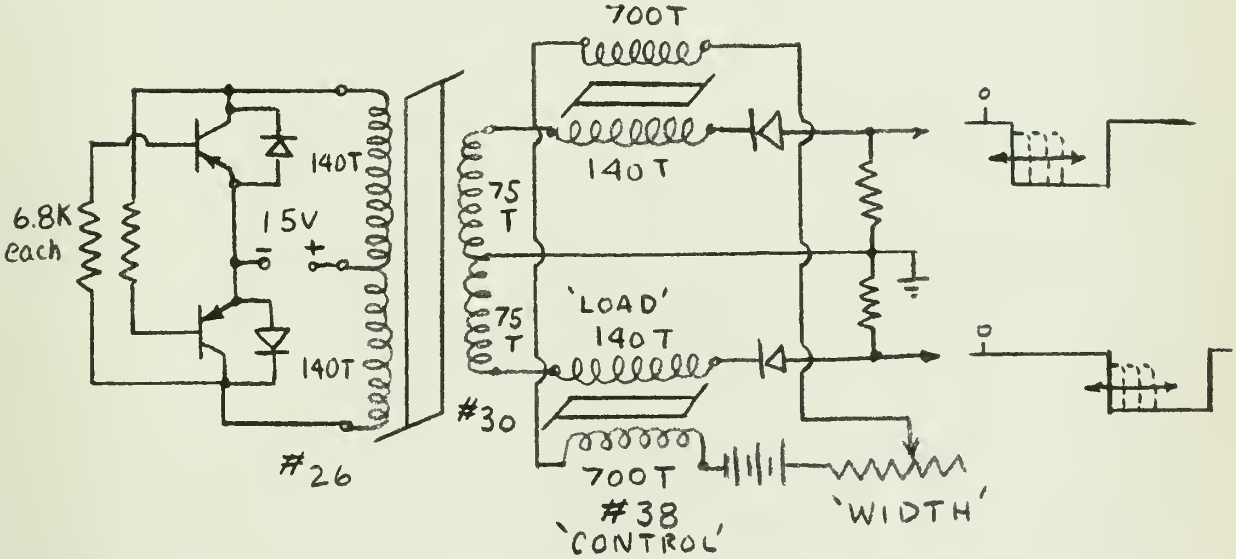


Fig. 12 Saturable-Core Oscillator with Width Modulation

When zero current flows in the control windings of the saturable reactors, the transformer output saturates the reactor cores almost instantly and the waveform is essentially unaltered. As current is increased via the 'Width' control,

a reverse biasing flux is set up in the reactor cores which must be overcome by the flow of square wave current in the load windings before the cores can be saturated. As a consequence, the leading edges of the square waves are delayed as shown at the right.

As the leading edges of the resulting square waves will be differentiated to initiate pulses for triggering the SCR drivers, a fast and clearly defined rise time is necessary. Unfortunately, the rise time in the original design was measured to be 34 microseconds; entirely too slow for the purpose. Two different reactor core materials were tried; Orthonol and HiMu80, each spirally wound of one mil tape. Rise time was essentially the same with both but was fast enough to serve as the input to a pair of push-pull switching transistors. These transistors are driven into saturation and give a rise time of two microseconds.

The variation of square wave width was observed to be relatively linear as biasing current(width control) was varied, and symmetrical in the sense that the two output waveforms were delayed the same amount. The battery and potentiometer used here for biasing the saturable reactors will be replaced in the final design by an input derived from an output-voltage error sensor.

The next step was to synchronize the saturable core oscillators by means of a series of short-duration pulses with an 800 cycle repetition rate. These pulses were supplied by test square-wave and pulse generators during laboratory development but will ultimately be derived by differentiating

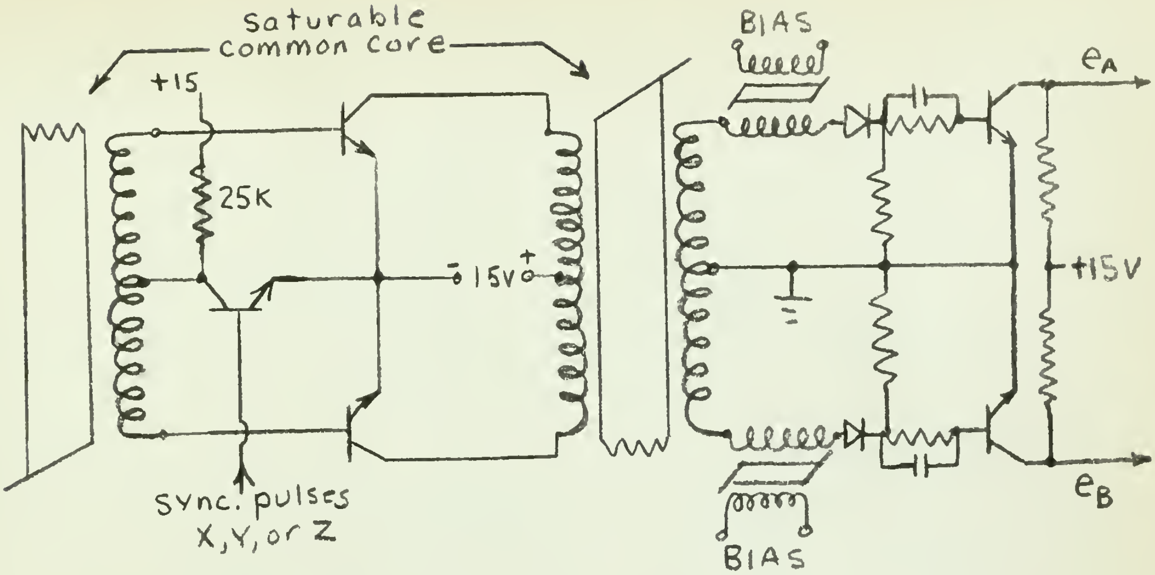


Fig. 13 Magnetic Pulse Width Modulator

800 cycle square waves, X, Y, and Z from the ring counter.

The method used was to add a synchronizing winding to the core of the transformer whose primary forms part of the oscillator circuit. Synchronizing pulses are supplied to this winding via a transistor amplifier stage.

The final magnetic pulse width modulator using the variable saturable reactor principle is shown in Fig. 13.

For the development of a sequence of four pulses which turn-on and turn-off the forward and reverse SCR's (via their drivers) to form the final output wave, e_A and e_B are counted down to provide A_1, A_2, B_1, and B_2; each containing alternate excursions of its parent wave form. See Fig. 14.

The logic circuitry for counting-down of e_A and e_B is very simple and is shown in Fig. 15. A 400 cycle square wave θ and its complement $\bar{\theta}$ (180 degrees) are used with e_A and e_B as inputs to four "and" circuits in which both inputs must be present simultaneously to get an output.

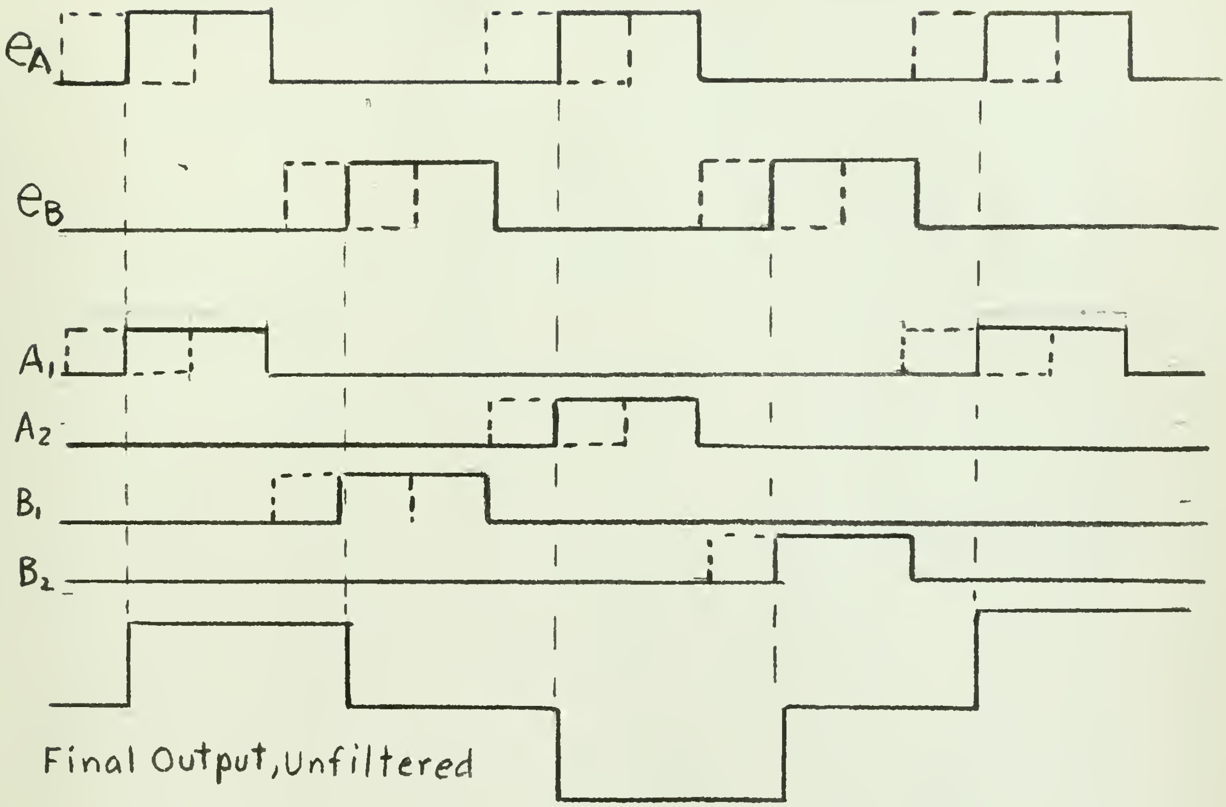


Fig.14 Wave Forms of Magnetic Pulse Width Modulator and Output Stage.

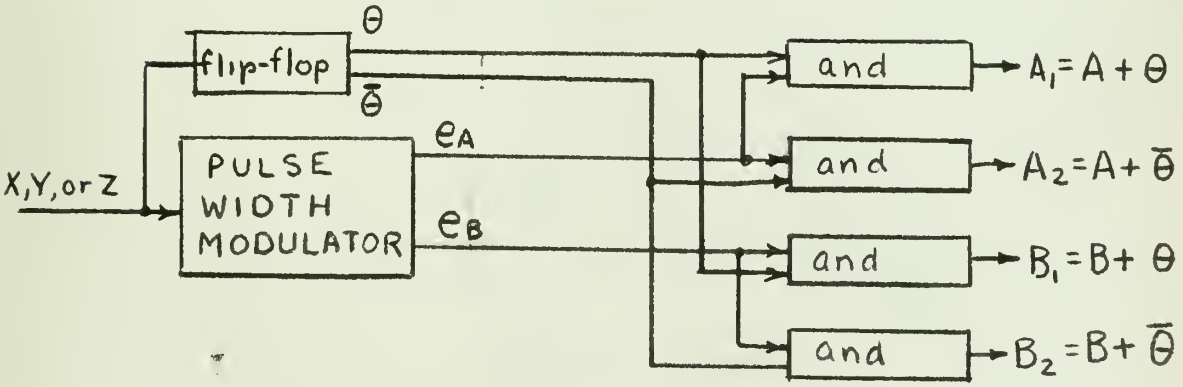


Fig.15 Digital Logic Separation Of Switching Pulses.

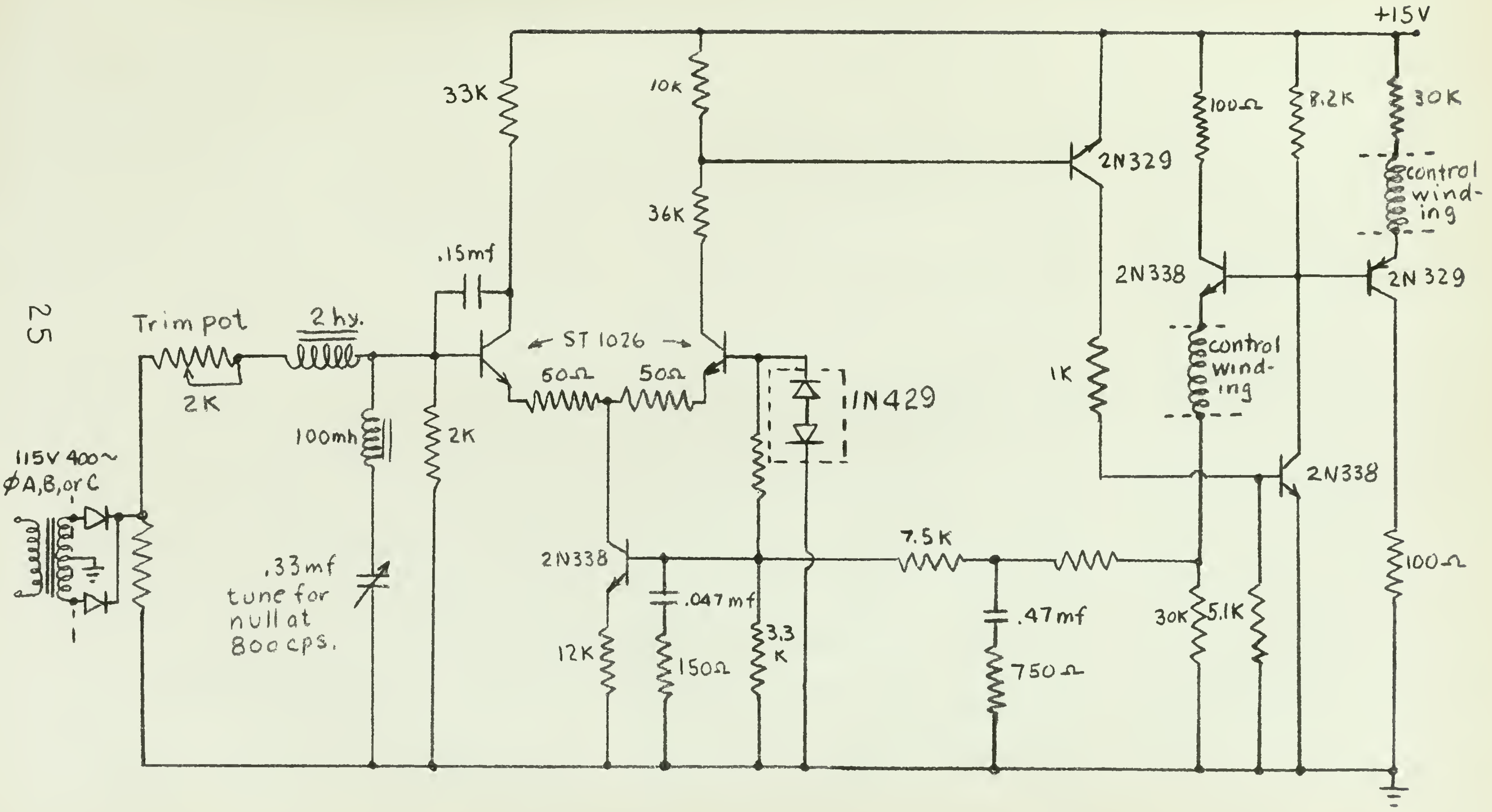


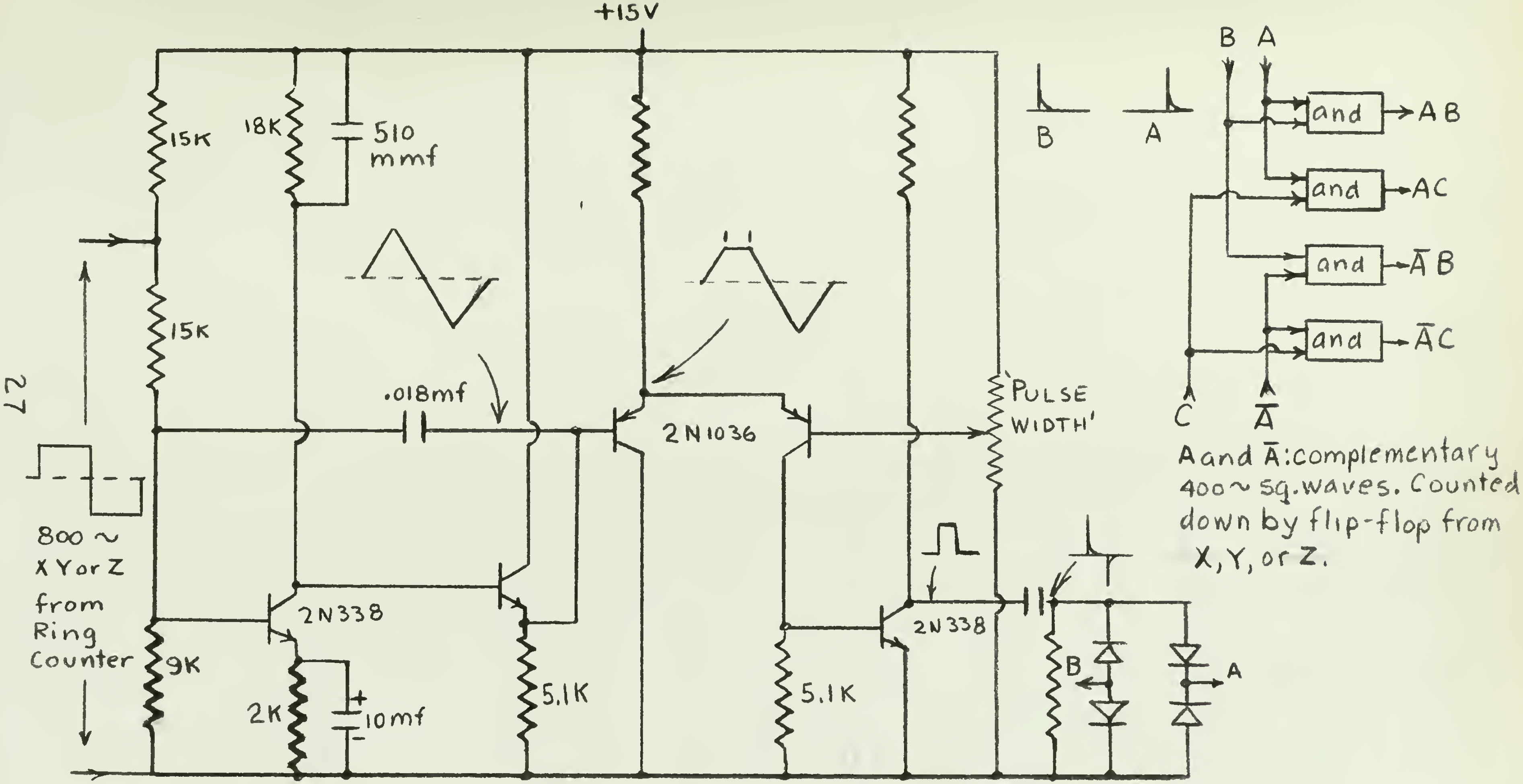
Fig.16 DC Feedback Amplifier for Magnetic Pulse Width Modulator

For the purpose of detecting deviations of inverter output voltage from the desired 115 volts and applying a compensating change of control winding current to the PWM, the amplifier circuit of Fig. 16 was designed. Sampled 115 volt, 400 cycle ac is rectified, filtered, and compared at reduced voltage to a zener-diode reference (1N429). Transistor amplifiers vary control winding currents in the saturable reactors of the PWM.

Adequate control of output voltage was achieved when the loop was closed but certain aspects of the magnetic pulse width modulator were not completely satisfactory. Some of these characteristics were as follows: (a) instability of keying of saturable-core square-wave oscillators, (b) asymmetry of the amount of advance versus delay of output trigger pulses as the control current was varied, (c) excessive power consumed, (d) excessive bulk and weight, and (e) excessive care required in matching of cores and windings of saturable reactors.

These drawbacks were not considered completely disqualifying, but concurrent development of an all-transistor width modulator showed sufficient promise to indicate its further investigation prior to attempting to improve the magnetic PWM.

The experimental circuit shown in Fig. 17 receives an 800 cycle square wave (X, Y, or Z) directly from the ring counter and integrates it into a very linear and symmetrical sawtooth wave. This sawtooth wave is applied to one of a pair of transistors (2N1036). To the second transistor of the pair, a variable dc level is applied. When the rising and falling



A and $\bar{A}$: complementary 400~ sq. waves. Counted down by flip-flop from X, Y, or Z.

Fig.17 Experimental Transistorized Pulse Width Modulator.

sawtooth voltage transits this variable dc level, a square pulse (straddling the sawtooth peak) is developed. Properly differentiated and subjected to the digital logic manipulation shown, the edges of this pulse serve as the trigger pulses for the output stage drivers.

The final circuit and its waveforms are shown in Fig. 18. It will be noted that a part of the digital logic circuitry indicated in Fig. 17 has been incorporated in this circuit. The remainder will appear in the output driver stage, or Blocking-Oscillator Driver, to be developed in the following section.

The dc feedback amplifier to be used with this transistorized PWM is shown in Fig. 19. Upon completion of this new transistorized version of the PWM, it was coupled to an output stage and feedback amplifier and the loop closed. Oscillation of the loop resulted for the first few trials, but it was possible to vary the loop transfer function by component changes and thus obtain stable operation.

Regulation of inverter output voltage by this latter system proves to be linear over a generous range of supply-voltage and load variations.

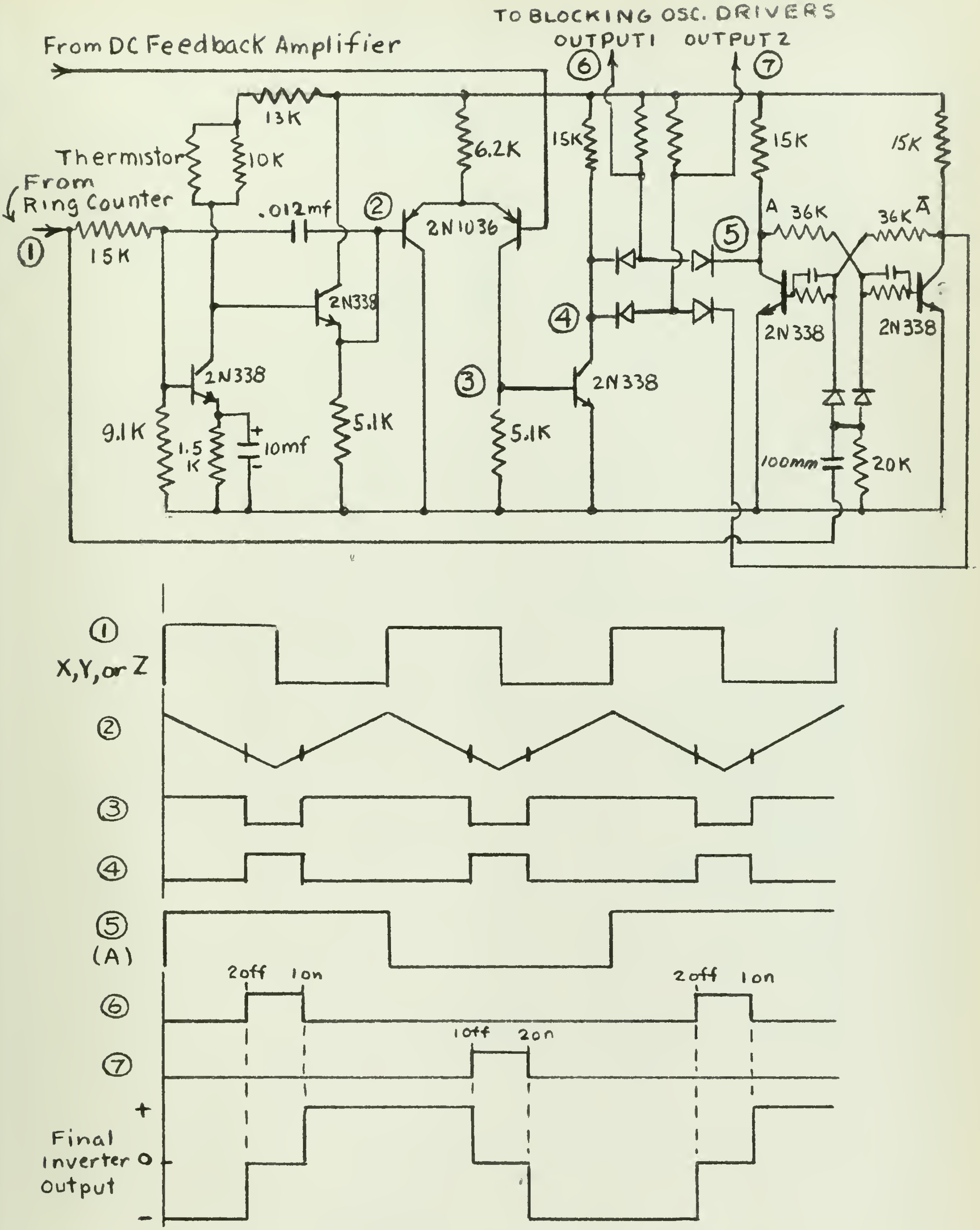


Fig.18 Transistorized Pulse Width Modulator and Wave Forms.

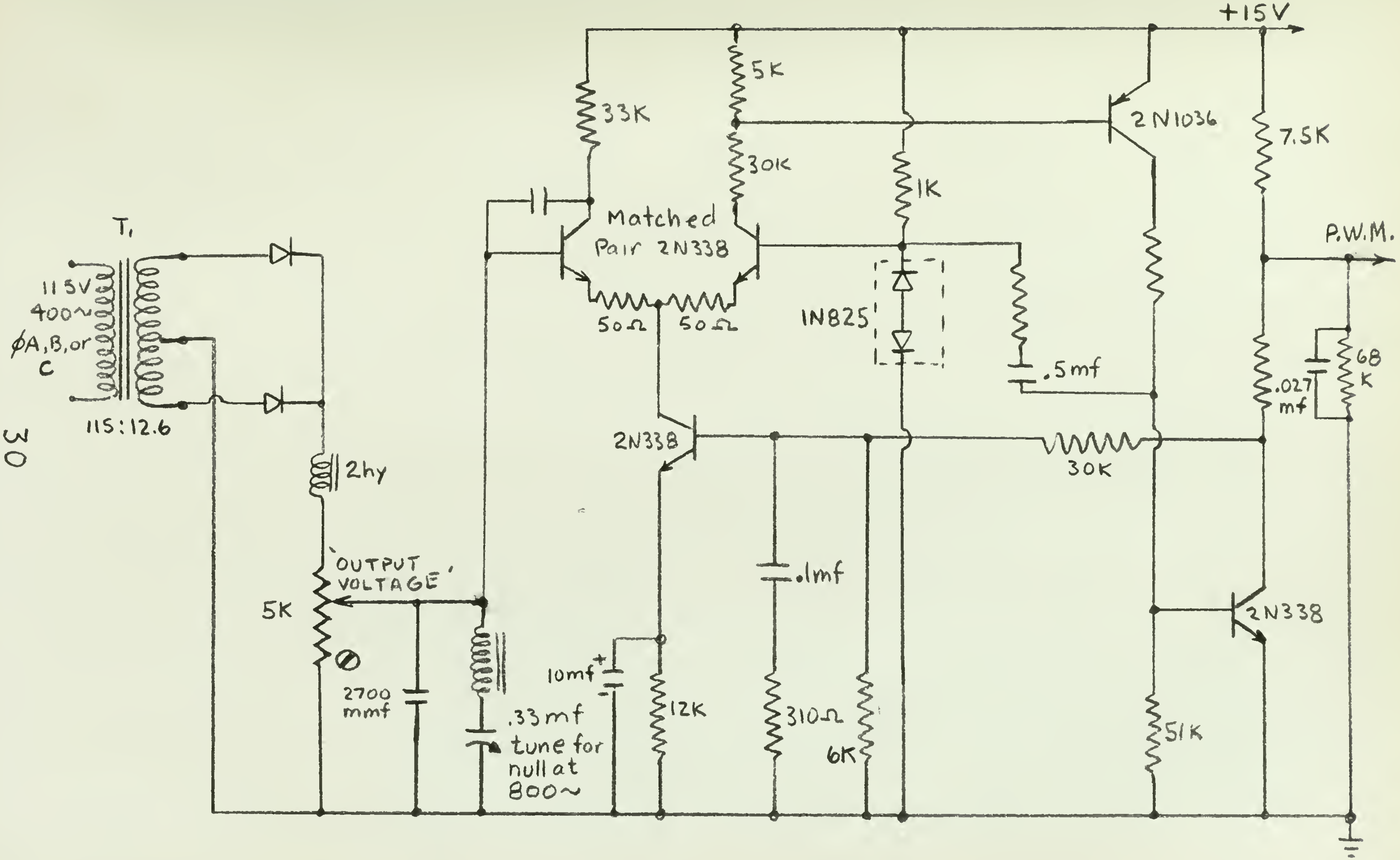


Fig.19 DC Feedback Amplifier for Transistor Pulse Width Modulator

V

Power Switching by Silicon Controlled-Rectifiers

The germanium power transistors used as switches in the commercial inverter tested in the early stages of this project were a serious source of power loss. At the heavy current flows encountered, appreciable power was dissipated in these transistors in spite of their low forward resistance. Other disadvantages are their need for considerable base drive power and their unfavorable temperature characteristic.

An attractive replacement for these transistors is the Silicon Controlled-Rectifier (SCR) announced during 1958 by General Electric. This is a four layer (pnpn), three junction, solid state device capable of performing many of the tasks of thyratrons and magnetic amplifiers.

Essentially the SCR is an ordinary silicon rectifier modified to block in the forward direction until a small signal is applied to its gate lead. After this signal is applied, the SCR conducts with forward characteristics similar to those of an ordinary rectifier and continues conduction *after* the signal is removed. The forward voltage drop is about 10% of that of a thyratron and its 'deionization' time is less by several orders of magnitude.

The theory of operation of the SCR is best described by considering it as a PNP and an NPN transistor pair with a common collector junction, (a) and (b) in Fig. 20. In transistor (a) α_1 is that fraction of 'hole' current injected

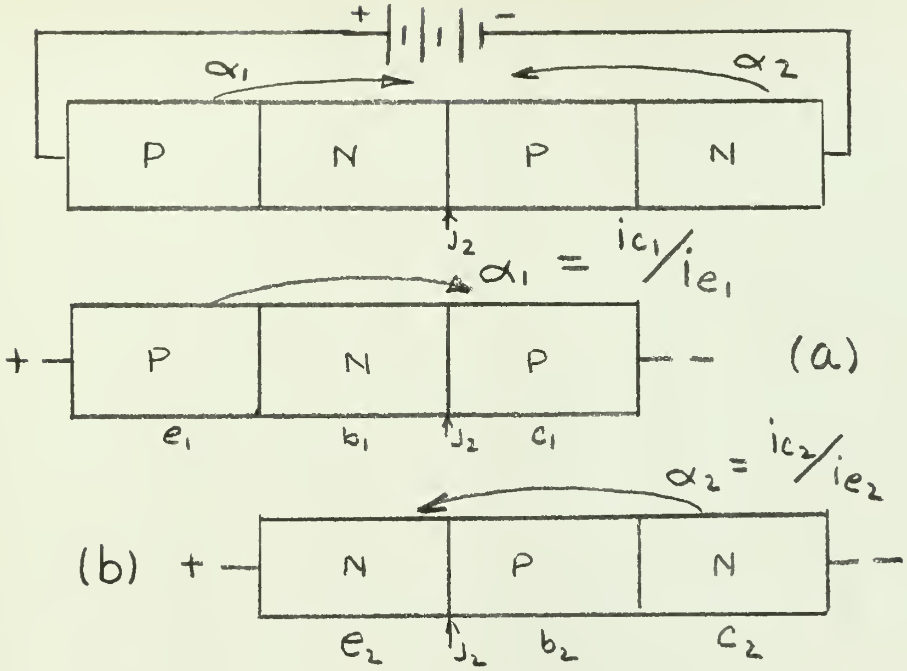


Fig. 20 Principles of SCR Operation

at the emitter e_1 which reaches the collector C_1 . Similarly, in (b) α_2 is the fraction of electron current injected at e_2 which reaches C_2 . The total current flowing in the pnpn structure is the sum of currents flowing in the individual transistor sections. The current crossing junction J_2 has three components: I_{α_1} = hole current from P end region, I_{α_2} = electron current from N end region, and I_{co} = leakage current. Since the total current at J_2 must be equal to the external current (I), a slight rearrangement shows that external current (I) is equal to :

$$I = \frac{I_{co}}{1-\alpha_1-\alpha_2}$$

If the values of α_1 and α_2 are such that their sum is 0.9, then the current flowing is ten times the leakage current. As the leakage current in a silicon pn junction can be made

very small, the total current will also be small and we have the 'off' condition of the SCR. However, if $\alpha_1 + \alpha_2 \approx 1$ the denominator is almost zero, the current is limited only by the external circuit, and the 'on' condition exists. Physically, in the 'on' condition the two center regions of the SCR are saturated with carriers; giving all three junctions forward biases. Hence, the entire potential drop across the SCR is about that of one forward-biased pn rectifier.

There are two mechanisms that may be used to increase the α's of the component junction transistors in order to turn on the SCR. These mechanisms are shown in Fig. 21. The current gain(α) increases slightly as the collector to emitter voltage(V_{CE})is increased, until a voltage is reached where the energy of carriers arriving at the collector pn boundary is sufficient to dislodge additional carriers; producing a form of avalanche breakdown analogous to a Townsend discharge in gases. This causes an increase in α with voltage increase as shown in Fig. 21 (a). In typical silicon transistors α is quite low at low emitter currents but increases fairly rapidly as emitter current(I_E) is increased. (Fig. 21 b). Both methods for increasing α may be used to turn on the SCR; the former by increasing anode to cathode voltage, the latter by introducing current at one of the bases (transistor action).

Fig. 22 shows typical voltage/current characteristics and operating regions of the SCR. In the forward-blocking region increasing forward voltage does not tend to increase current until the point is reached where avalanche multipli-

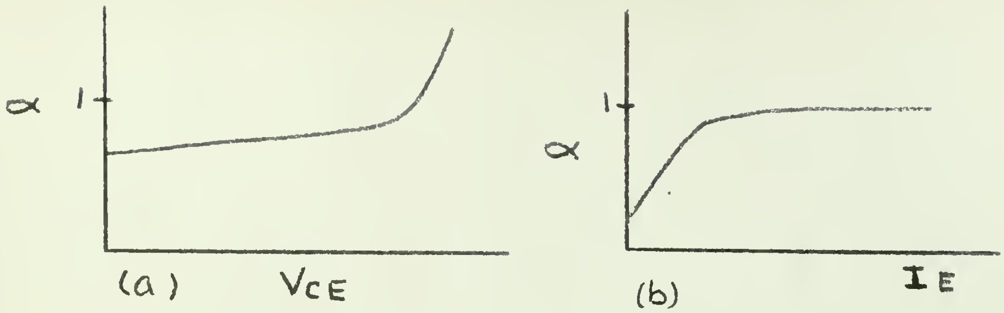


Fig.21 Functional Characteristics of Silicon Controlled-Rectifier

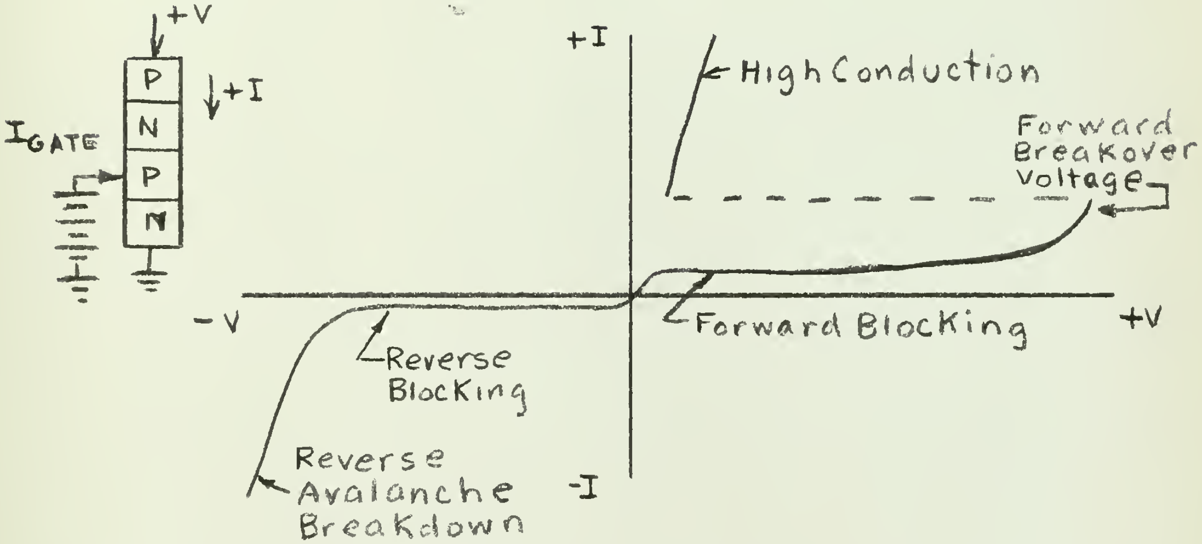


Fig.22 Operational Characteristics of Silicon Controlled-Rectifier

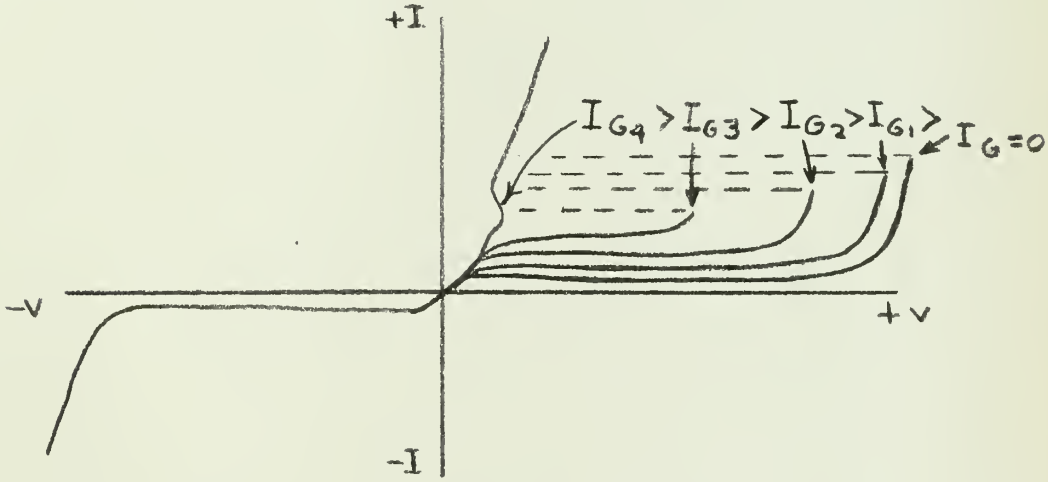


Fig.23 Typical Operation of Silicon Controlled-Rectifier

cation begins to take place. Beyond this point current increases rapidly until total current through the device is sufficient to maintain the sum of the α's equal to, or greater than, one. At this point the SCR goes into the high conduction region; provided that current through it remains above the minimum 'holding' value. If current drops below the 'holding' level the SCR reverts to the forward blocking region. In the reverse direction the SCR has essentially two back-biased pn junctions in series and thus has characteristics similar to those of back-biased silicon rectifiers. For increasing values of gate current, the region of characteristics between 'forward-blocking' and 'holding-current' is narrowed and forward-breakover voltage is reduced down to a point where the entire forward-blocking region disappears. At this point the voltage/current characteristics of the SCR are merely those of a pn rectifier. Fig. 23 illustrates the conditions for several values of gate current.

In typical operation the SCR is biased well below forward-breakover voltage. Triggering is accomplished by injecting current into the 'gate' lead which increases current flow through the device by transistor action. Both alpha's are increased, being current sensitive.

By proper design it is possible to make the sum of the alpha's greater than one by increasing the current through the gate by a small amount. This lowers the breakover voltage below that impressed across the device, thus allowing the use of a higher forward breakover voltage than would normally

be encountered in the circuit, and the use of only moderate trigger power to start the high-conduction mode. Again, when the gate has triggered the SCR into high conduction, turn-off can only be achieved by reducing main current below the holding current level.

The gate-cathode voltage/current characteristics are those of a forward biased pn junction diode. Since the increase of alpha is achieved by an increase of current, this is a 'current-triggered' device, as contrasted to the voltage-triggered gas thyratron; thun a low impedance source for triggering must be used.

From the specifications of the various types of SCR available, the Type C35A was selected as being adequate for the switching problem at hand. C35A ratings of most interest are: (a) average forward current: 0 to 16 amps, (b) peak Inverse Voltage: 100 volts, (c) maximum gate voltage and current to fire: 3 volts and 25 ma., (d) average gate power: .5 watts, (e) typical turn-on and turn-off times: 1 to 4.5 μ sec. and 10 to 20 μ sec., respectively.

Turn-on pulses must have a duration sufficient to allow anode current to build up to the holding current level and are simply obtained with a blocking oscillator. Turn-off pulses are a more serious problem, it being necessary to reduce anode voltage to zero, or even to a negative value, for a considerable longer time. When the SCR is in the conducting state, each of the three junctions are in a condition of forward bias and the two base regions are heavily saturated with holes and electrons (stored charge).

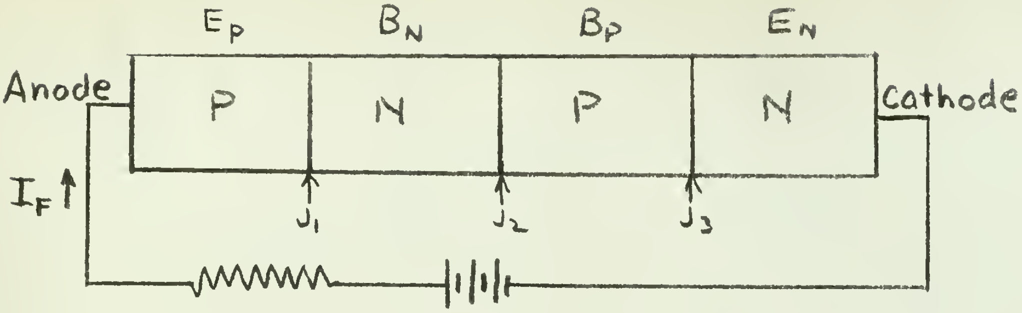


Fig. 24 SCR Biased in Conducting State

Minimum turn-off requires application of a reverse voltage which causes holes and electrons in the vicinity of end junctions J_1 and J_3 (see Fig. 24) to diffuse to the junctions, resulting in a reverse current in the external circuit. The voltage across the SCR will remain at about +0.7 volts as long as an appreciable reverse current flows. After the holes and electrons in the vicinity of J_1 and J_3 have been removed, the reverse current will cease and J_1 and J_3 will assume a blocking state. The reverse voltage across the SCR will then increase to a value determined by the external circuit. Recovery of the SCR is still not complete since a high concentration of holes and electrons still exists in the vicinity of J_2 . This concentration decreases by the process of recombination in a manner largely independent of external bias conditions. When it reaches a low value, J_2 regains the blocking state and forward voltages, if less than the forward-breakover value, may be applied without causing turn-on.

Turn-off circuits suggested by the manufacturer included shunt and series capacitor turnoff circuits and a shunt transistor turnoff. Of these, the shunt capacitor turnoff, shown

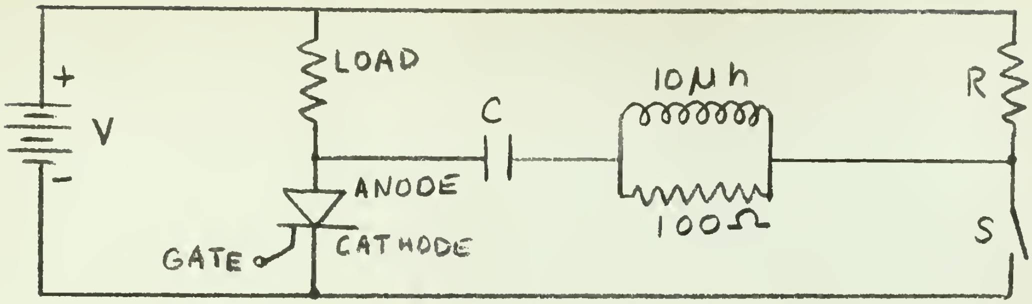


Fig. 25 Shunt Capacitor Turn-off Circuit

in simplified form in Fig. 25, seemed best adapted.

While the SCR is in the conducting state, source voltage V appears across the load and charges capacitor C through resistor R so that the right side of C is positive with respect to the anode. When turn-off is desired, switch S is momentarily closed, connecting the positive terminal of C to the cathode. This reverse biases the SCR and diverts load current long enough for the SCR to regain the forward blocking state. With resistive loads I reaches zero as soon as the voltage on C has reversed and reached the supply level. The LR network in series with C limits reverse recovery current through the SCR to reasonable levels without inducing excessive voltage upon recovery. In a practical circuit S is replaced by another SCR.

A complete output stage for one phase was assembled including two switching SCR's, a center-tapped transformer, and the associated turn-on and turn-off (shunt capacitor type) circuitry. Testing revealed that transients due to switching of either SCR adversely affected the functioning of the other and that turn-off was not sufficiently reliable. An improved

circuit shown in Fig. 26 incorporates the following added features: (a increased energy available for turn-off; gained by use of resonant charging of the shunt turn-off circuit, (b) limiting of the core resetting surge, and, (c) coupling of turn-on and turn-off pulses from separate drivers via pulse transformers.

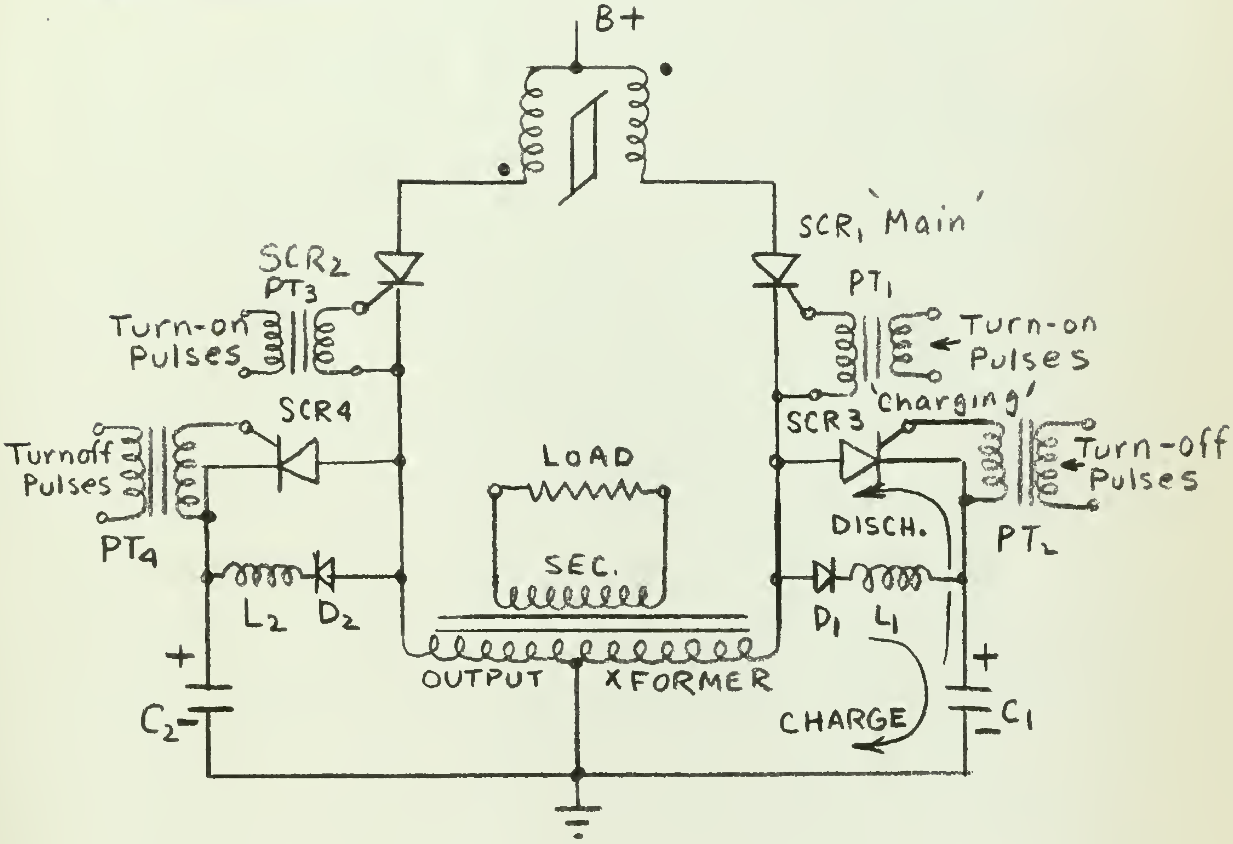


Fig. 26 Experimental Output Stage

The sequence of operation of one side of this output stage commences with a short pulse, via pulse transformer PT$_1$ applied to the gate of main-switching SCR1 to turn it on. Due to the low resistance of SCR1 while conducting, B+ appears across the right half of the output transformer primary supplying the load and charging turn-off capacitor C$_1$.

C_1 charges to 2B+ by resonant charging in series with inductor L_1 and diode D_1.D_1 and turn-off rectifier SCR3 effectively open to hold the charge on C_1 until a turn-off pulse viaPT_2 fires SCR3 ,thus providing a low resistance path from C_1 to SCR1.The charge on C_1reverse biases SCR1 until it regains the forward blocking state.The left side of the circuit functions in a similar manner to form the opposite excursion of the desired delayed square wave output.It is to be noted that the value of 10 mfd.for C_1 and C_2exceeds the calculated minimum value for adequate reverse biasing. This added measure of safety is desired to preclude the possibility of both main switching rectifiers firing at the same time.

Reliability of turn-on and turn-off of this circuit was found to be excellent under fixed load but suffered when the load was varied over the 10 to 100% range.To solve this problem the inductor in the resonant charging circuit was placed on the same core with a winding in series with the output transformer primary.Now, by autotranformer action, the charge on the turn-off capacitor automatically adjusts to varying loads and provides the extra energy required to achieve turn-off when the main SCR is conducting heavily.Diodes $D_1$and D_2 were replaced by 'charging' rectifiers(SCR5 and 6).These new SCR's are provided with their own isolated gating pulses from the blocking oscillator drivers.

The final output stage is shown in Fig.27. At time t_1 SCR's 1 and 5 turn on;SCR5 turns off when C_1 becomes charged. At t_2 SCR3 turns on,allowing charge on C_1 to back-bias SCR1

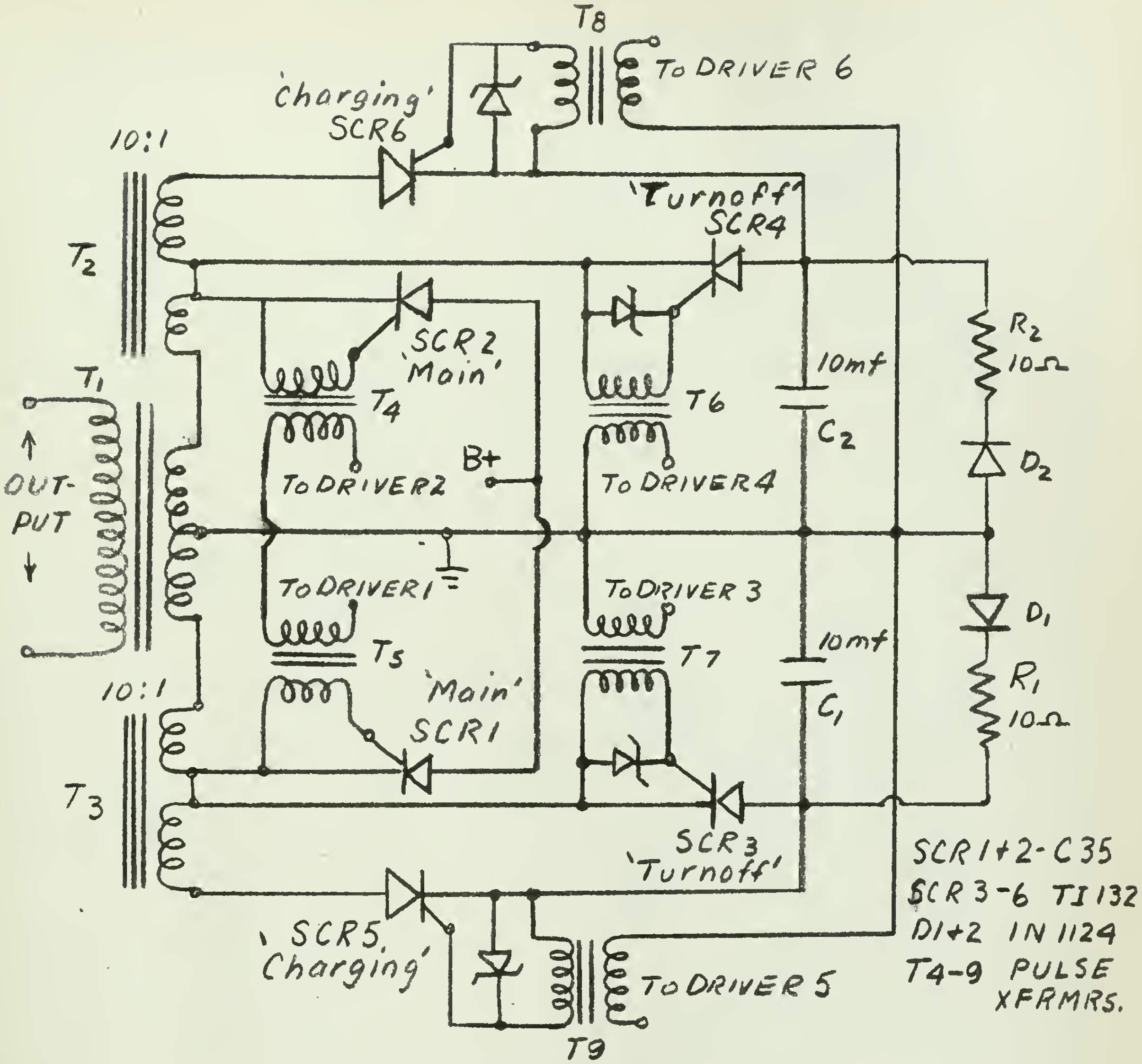


Fig.27 Single Phase Output Stage

and turn it off; SCR3 turns off when C_1 has discharged. At t_3 and t_4 SCR's 2,4, and 6 function in a similar sequence to form the negative excursion of the wave.

Interposed between the pulse width modulator and the output stage are two blocking oscillator drivers, one of which is shown in Fig.28. These drivers receive outputs one and two from the PWM's and generate the turn-on, turn-off, and turn-off circuit charging pulses required by the output stage.

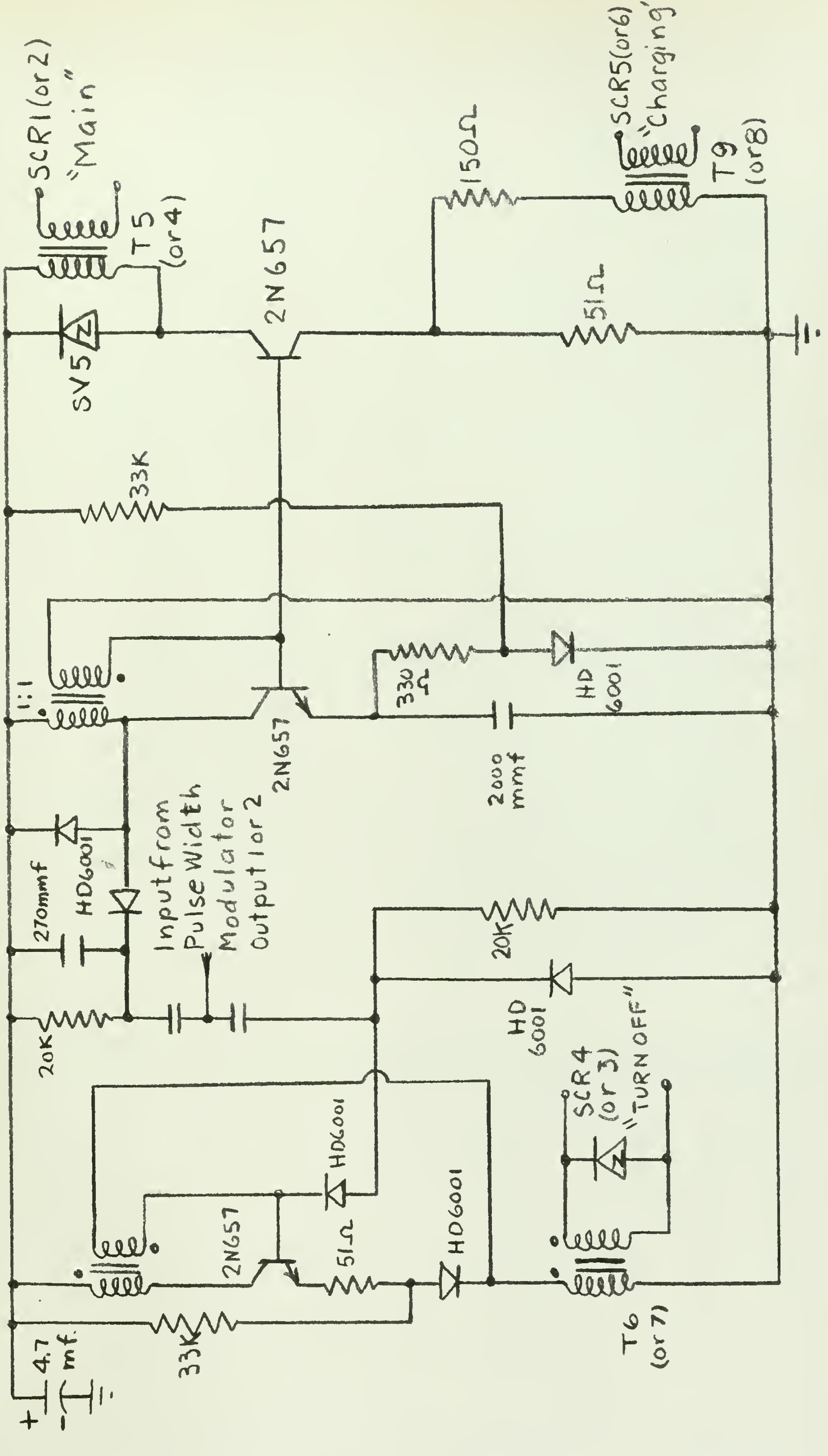


Fig. 28 Blocking-Oscillator Driver.

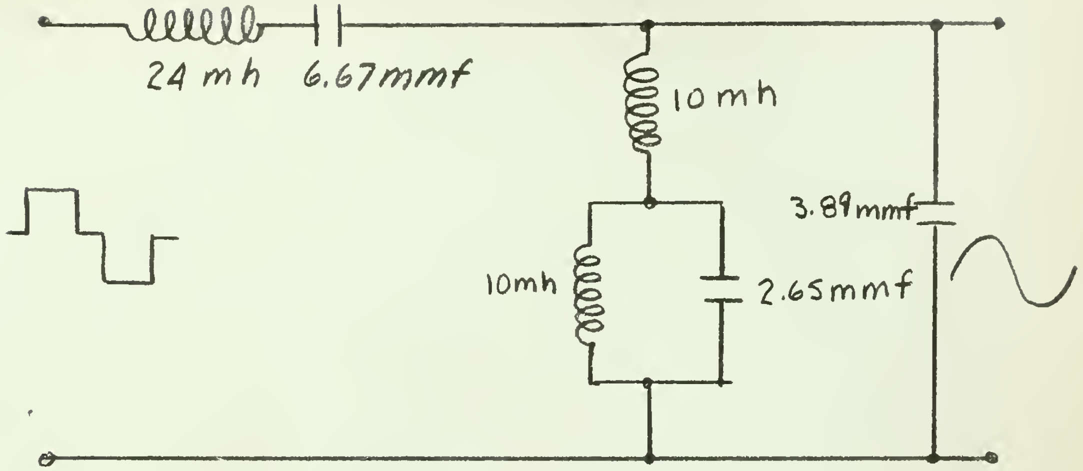


Fig. 29 Output Filter

Filtering of the delayed square-wave from the output stage is performed by the filter shown in Fig. 29.

A complete single-phase system including clock, ring counter, pulse width modulator, blocking oscillator drivers, output stage, filter, and feedback amplifier was assembled and tested for efficiency. Results are shown in the following table and in Fig. 30.

% Load	R Load	V Out	V In	I In	P Out	P In	P Loss	Eff.
100	74	114.3	30.3	7.5	176.6	227.3	50.7	77.7
90	83	115.2	29.8	6.9	159.0	205.6	45.7	77.8
80	93	114.9	29.1	6.25	142	181.9	39.9	78.1
70	108	114	28.2	5.4	120.3	152.3	32	79
60	128	114.5	27.7	4.7	102.4	130.2	27.8	78.7
50	154	115	27.2	4.07	85.9	110.7	24.8	77.6
40	193	115.6	26.7	3.4	69.2	90.8	21.6	76.2
30	255	114.6	25.7	2.68	51	68.9	17.9	74
20	388	114.9	25.2	2	34	50.4	16.4	67.5
10	782	115	24.5	1.35	16.9	33.1	16.2	51.1

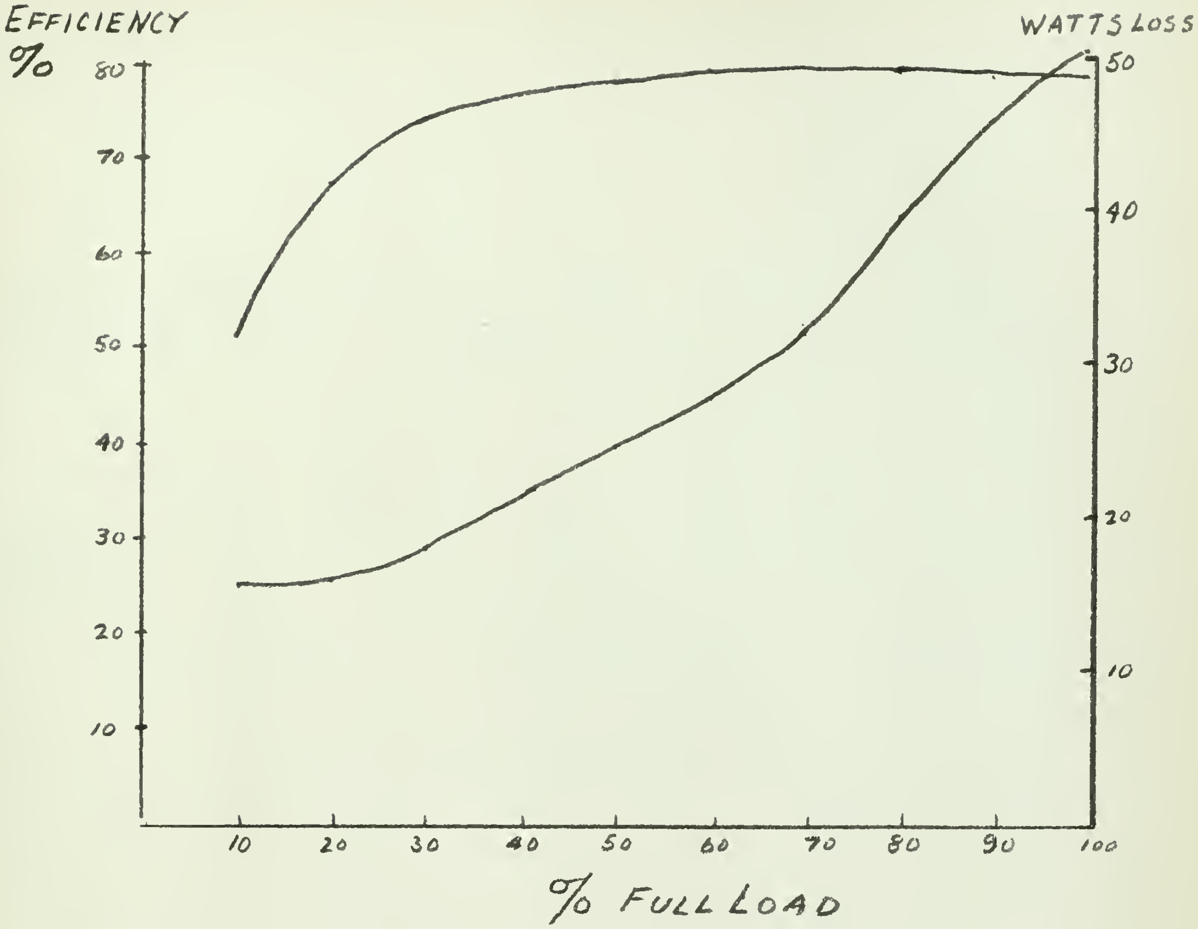


Fig. 30 Curves of Efficiency and Power Loss Versus Load

Efficiency attained remains below the specified 85%. Some improvement may be made by optimizing various component values but the main source of loss is believed to be due to a failure to achieve the delayed square wave form, as shown in the waveforms in Fig. 31. The waveform at the output transformer secondary should resemble the delayed square wave very closely in order to achieve the efficiencies found by Fourier analysis. Note that this waveform is worse at low load.

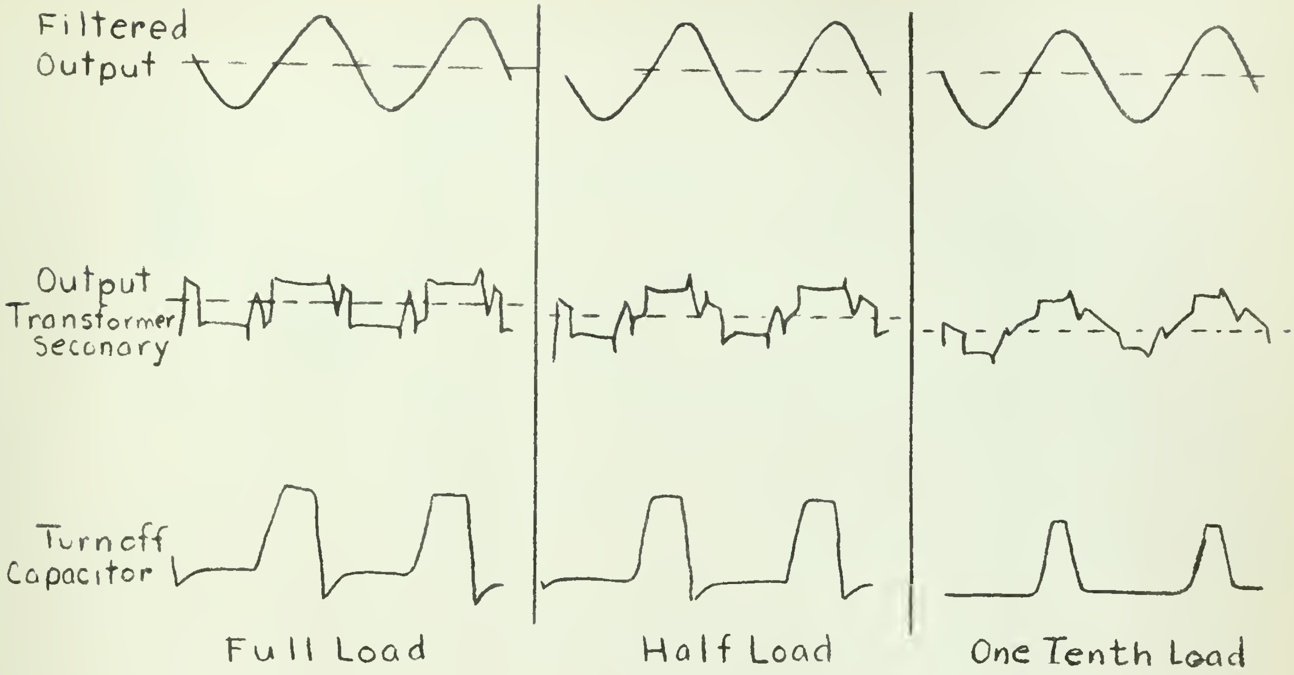


Fig. 31 Output Stage Waveforms

VI

Short Circuit Protection

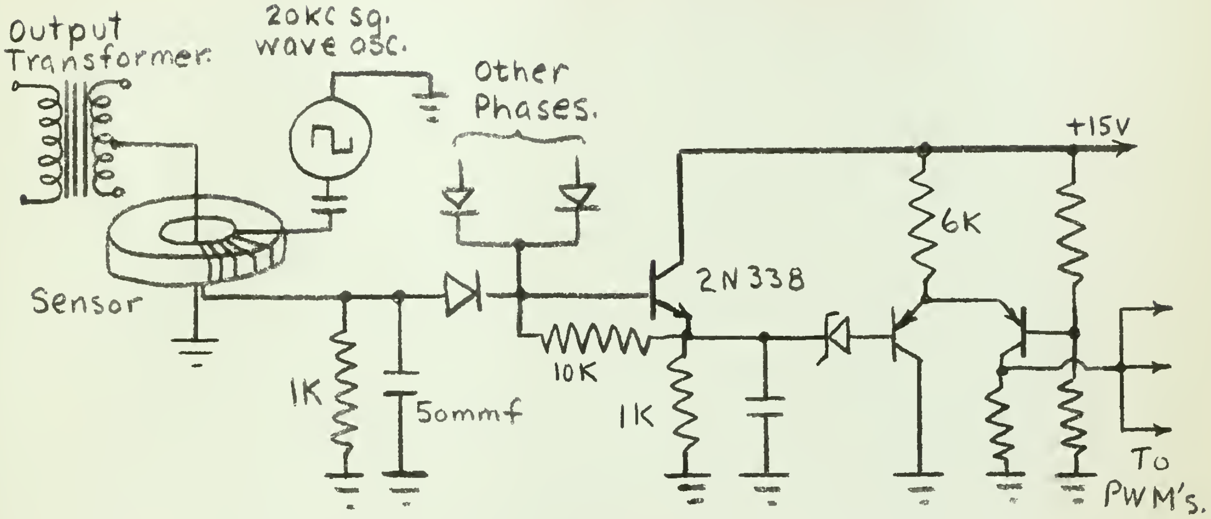


Fig. 32 Short Circuit Protection Circuit

Design specifications require that the inverter be protected against short circuits on any one, two, or all, phases. A logical approach to this problem is to utilize the features of the existing pulse width modulator. This may be done by injecting an overriding signal from an overload current sensor into the PWM to cause a quick shift to the minimum pulse width state. Output current is thus limited to a level which prevents damage to any component but the inverter stays 'alive'; ready to resume operation when the short is removed.

The best sampling point for load current is the lead to the output transformer center tap. Use of a dropping resistor as a sensor would entail power dissipation. The device used here is somewhat similar to a current transformer for ac ammeters. A small saturable toroidal core is slipped over

the center-tap lead. Through a coil on this core is passed a 20 KC square wave from a small transistorized oscillator. As the direct current through the center-tap lead increases, the flux in the sensor, and thus its impedance, varies. The drop across a resistor in series with the sensor winding is compared with a fixed voltage level representing some predetermined overload current (15 amps here). When this level is exceeded in any one or more phases, all Pulse Width Modulators receive an input which overrides the normal voltage regulation signals and cause their immediate shift to the minimum pulse width condition. This circuit is shown in Fig. 32.

VII

Conclusions

Although the authors Industrial Experience Tour ended before completion of this design project, the main operating principles have been adequately proven and many of the circuits established in their final form. It is the opinion of the author that design specifications will be met and that the completed device will represent a significant advancement over similar inverters now available.

It is the current feeling in the design group that the delayed square wave synthesis of a sine wave will have to be abandoned in favor of an eight step waveform as shown in Fig. 33.

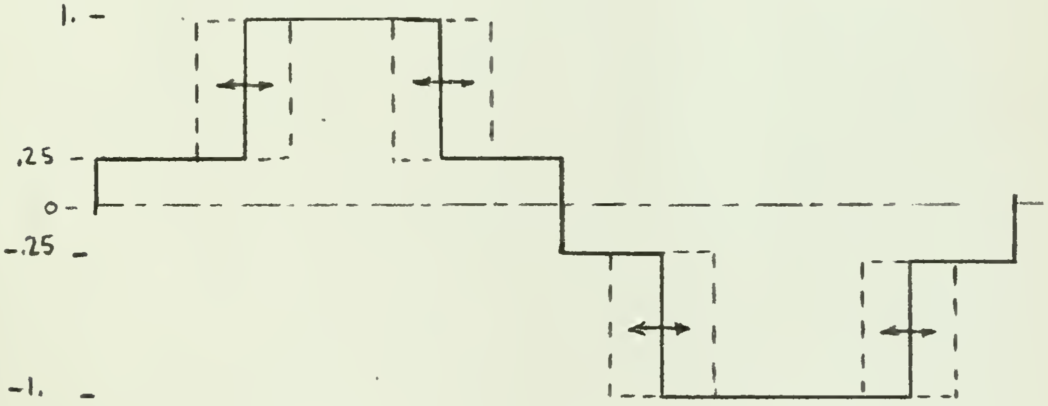


Fig. 33 Eight Step Wave Syntheses

This wave eliminates the periods when no SCR is firing and thus presents a more nearly constant impedance to the filter. Also, it is a closer representation of a sine wave, having less harmonic content to be lost in filtering.

An increase in the number of components and in circuit

complexity will ensue, unfortunately, but not to the extent that existed in the early twelve-step wave.

An overall block diagram of the inverter in its present state of development is shown in Fig. 34. Discussion of the input filter and regulated +15 volt control-circuit power supply have been omitted due to their relatively conventional design.

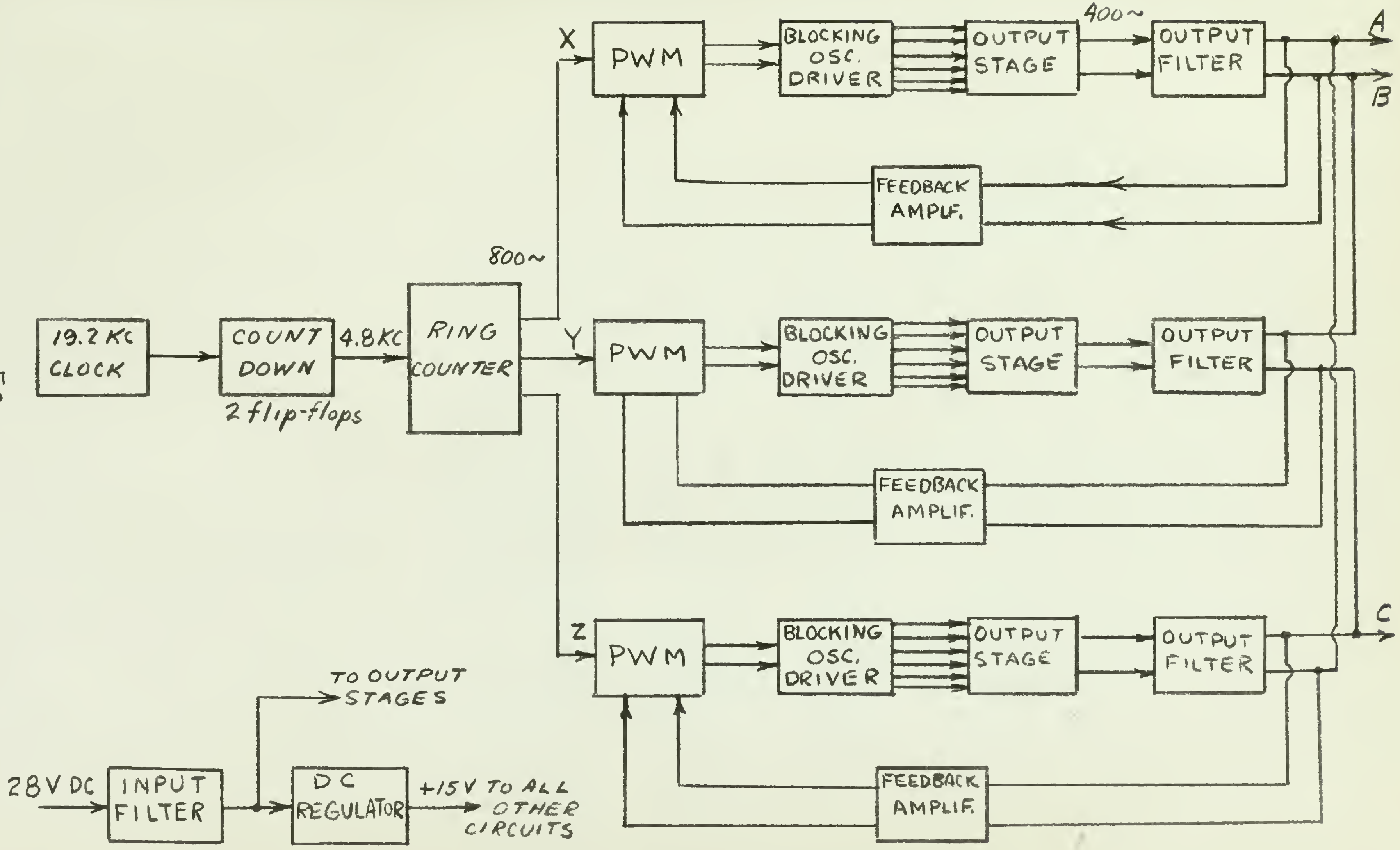


Fig 34. Overall Block Diagram

Bibliography

1. "Notes on the Application of the Silicon Controlled-Rectifier". Semiconductor Products Department, General Electric ECG-371-1 December, 1958
2. H. W. Collins "Magnetic Amplifier Control of Switching Transistors", AIEE Transactions. Vol. 75, Part 1
3. Ringelman and Fenarolli "Simple Reactor Circuit, Its Operation and Mode Transition". AIEE Transactions. January, 1957
4. Bud Tomer "Transistor Power Supplies". CBS-Hytron
5. D. A. Williams "Saturable Core Transformer Design".
6. H. F. Storm "Magnetic Amplifiers".
7. J. H. Walker and Max Frank. "Design Methods for Magnetic Amplifiers and Saturable Reactors". WADC Tech. Report 56-231, Astia AD110431
8. R. J. Stewart "Type VI Inverter Development Reports" of 8 May, 29 June, 7 August, 9 September and 9 October, 1959. (A Lockheed Intra-departmental report)

thesA7258
Digital wave synthesis and pulse width m
3 2768 001 00643 0
DUDLEY KNOX LIBRARY